

**FIG. 3**

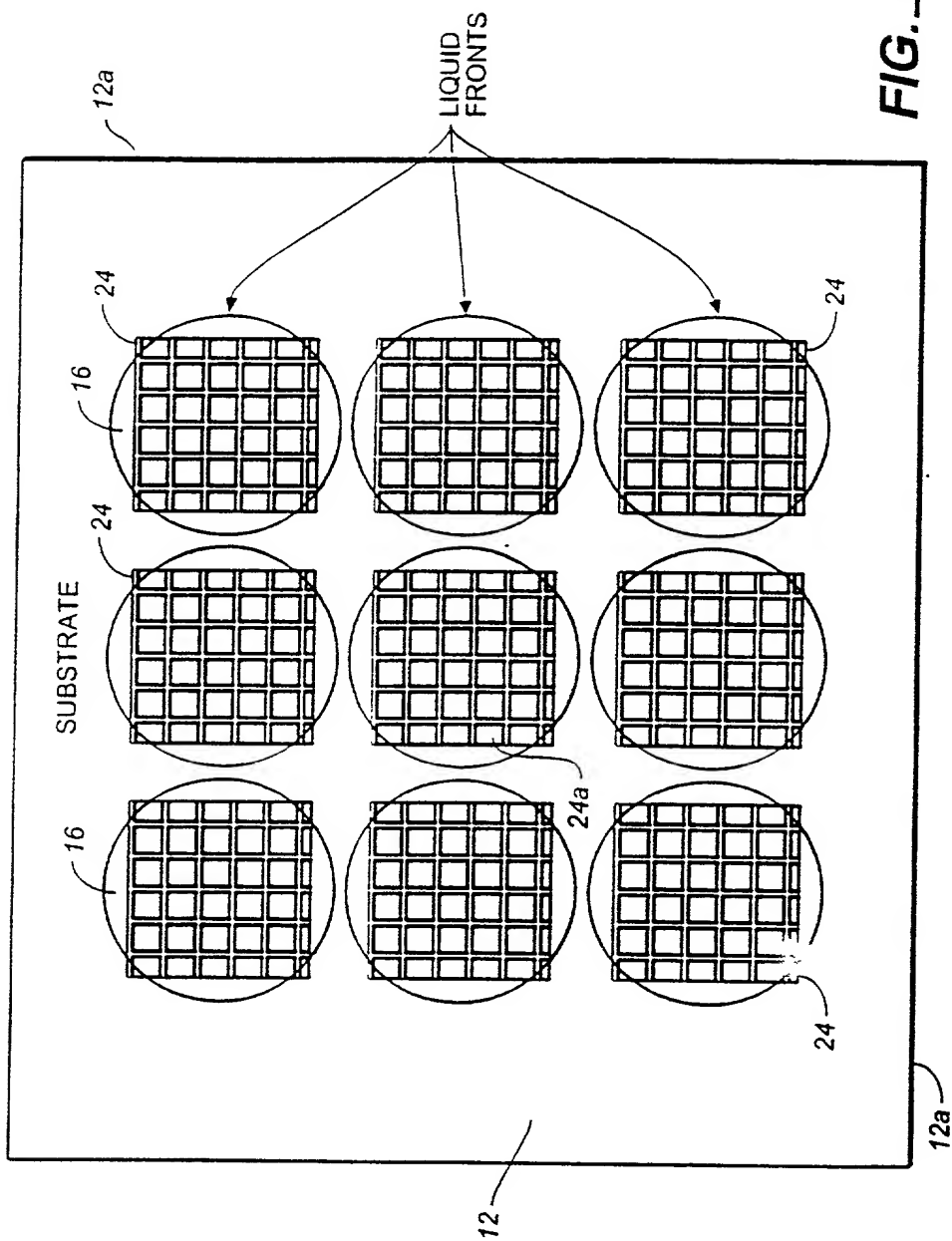
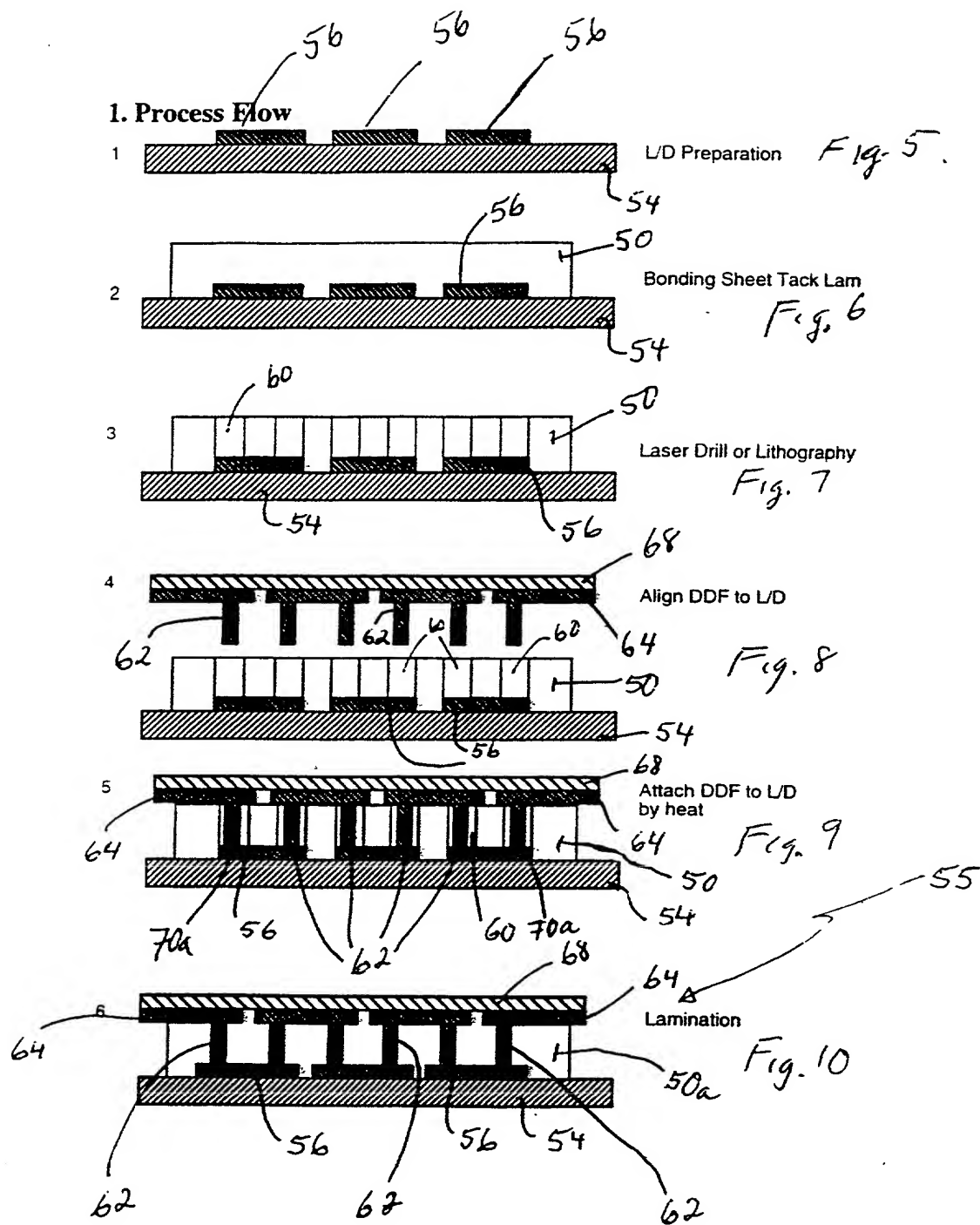
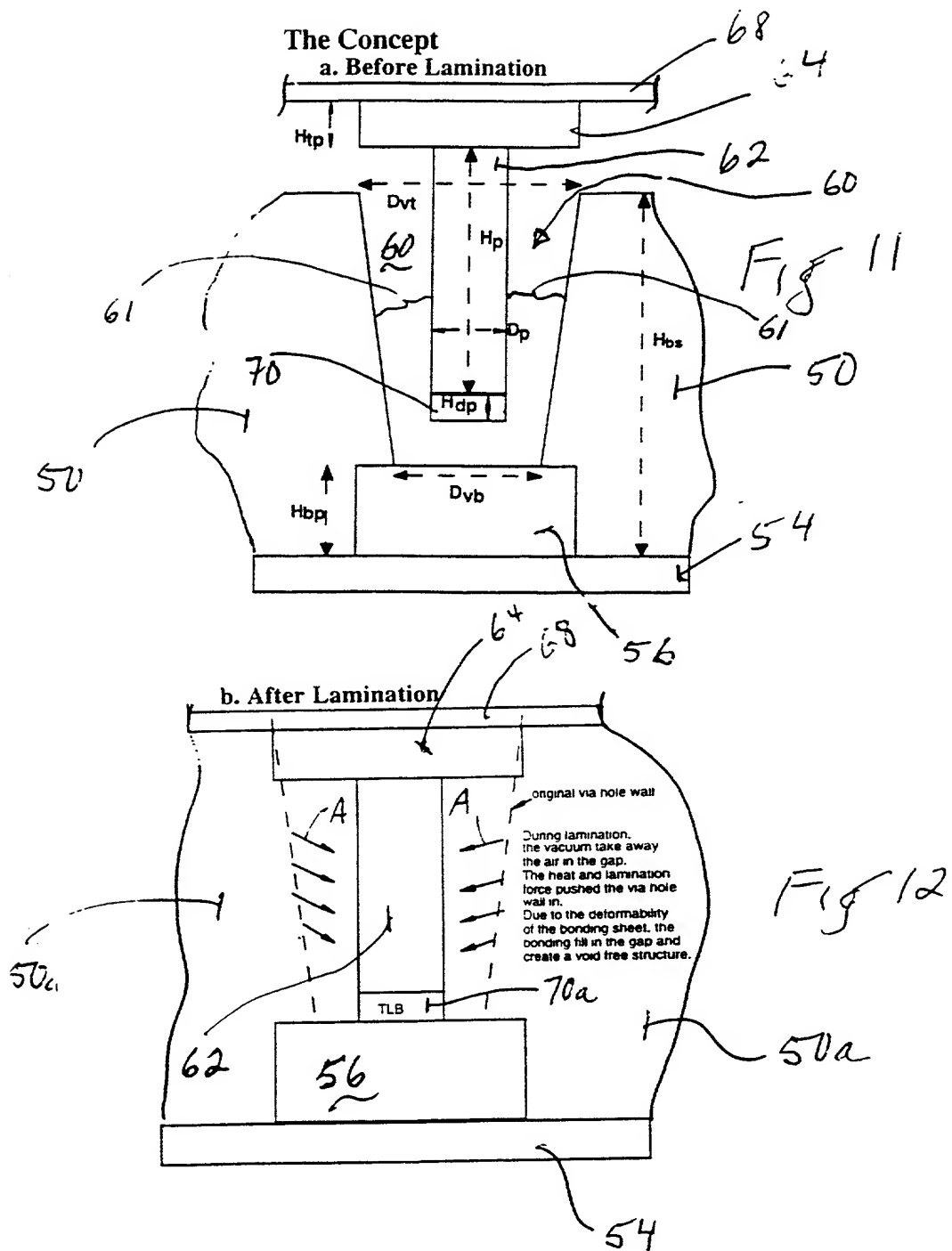


FIG. 4

10065498 020100





10064936 020102

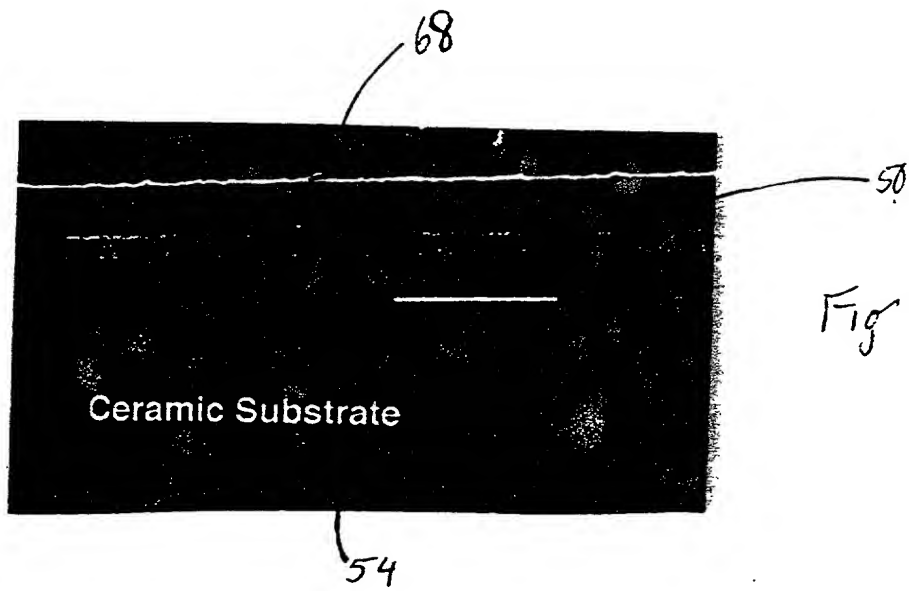


Fig 13

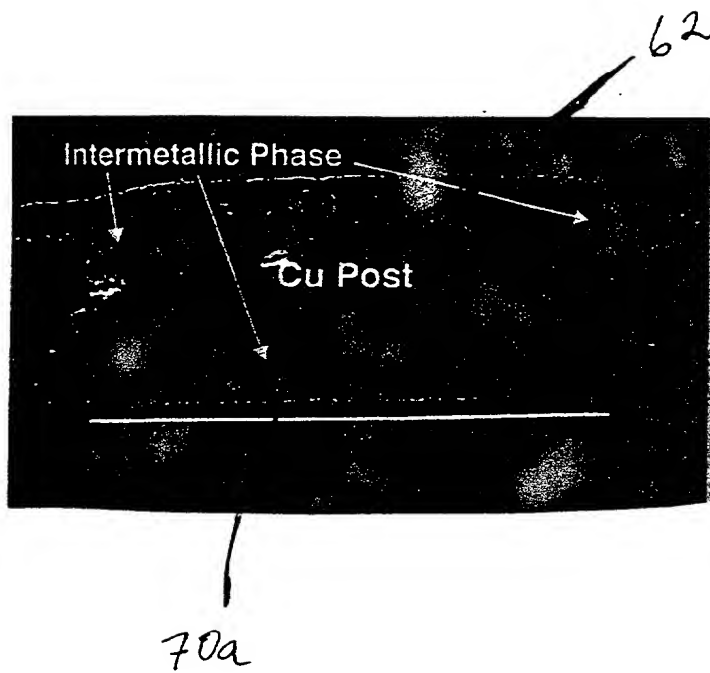
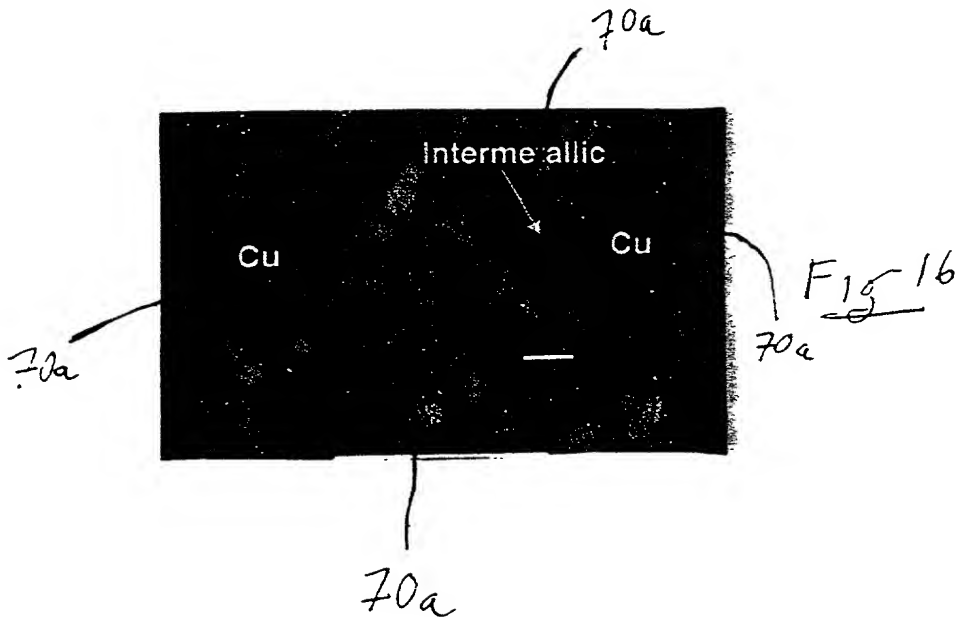
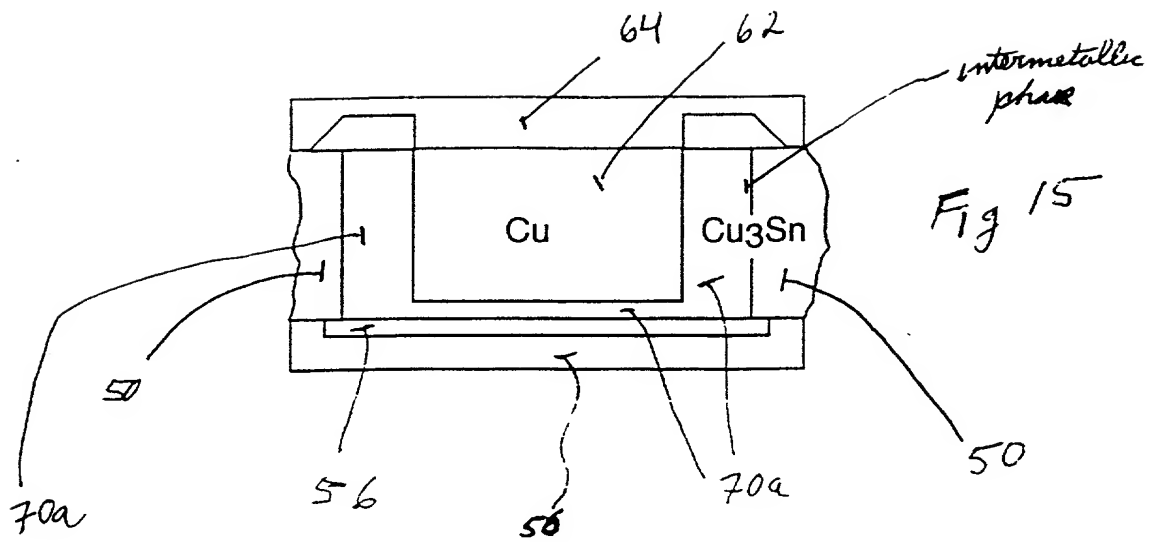
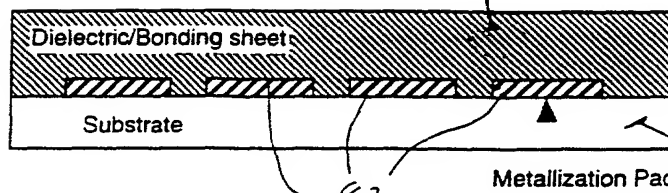


Fig 14

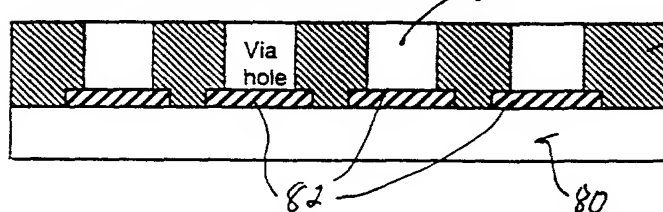
10055495 020102



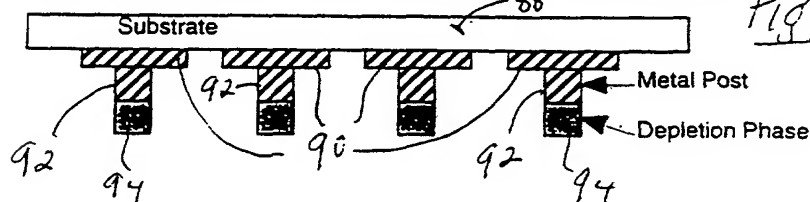
Tack lam the bonding sheet onto bottom substrate with metal pattern



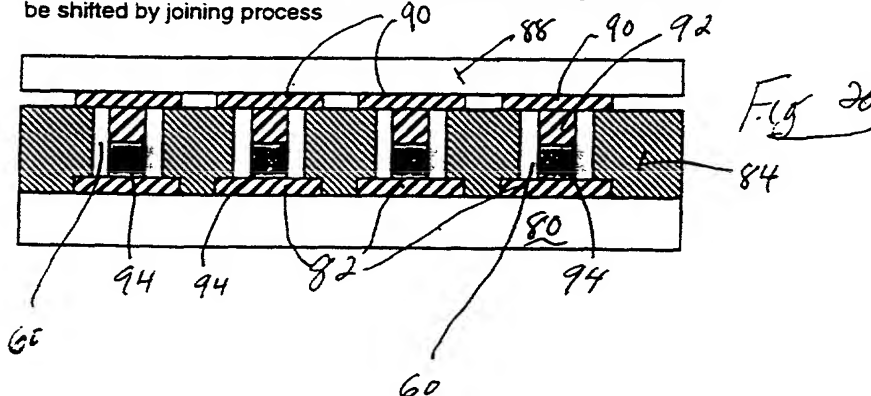
Laser drill via holes on top of metal pad



Top substrate has metal post and depletion phase metal deposited



Top substrate is aligned to the holes on bottom substrate and Laminated under pressure, temperature and in certain period of time. Because the post is anchored by the via hole, the alignment will not be shifted by joining process





After lamination at suitable temperature for both bonding sheet and Transient Liquid Alloy Joints, the final structure has a filled via with metal post embedded inside intermetallic wall.

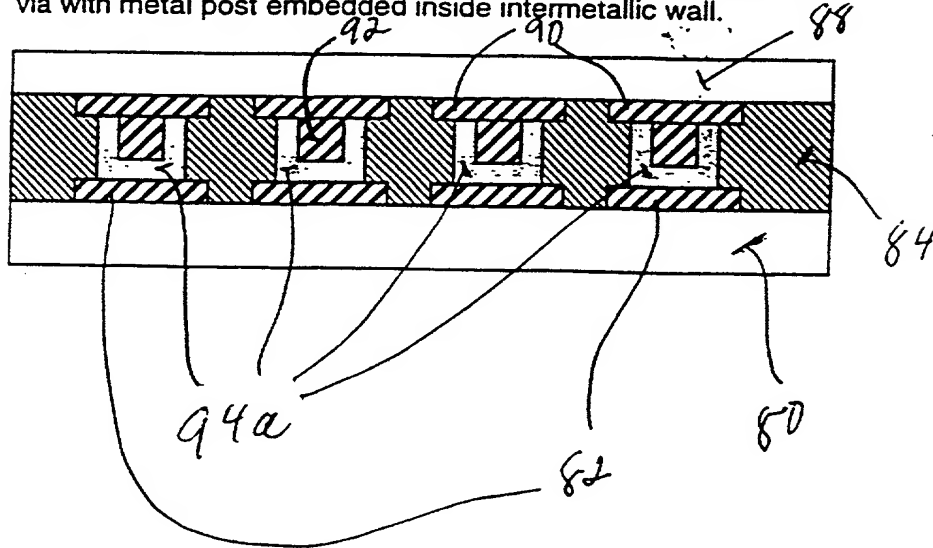


Fig 21

201003 5515001

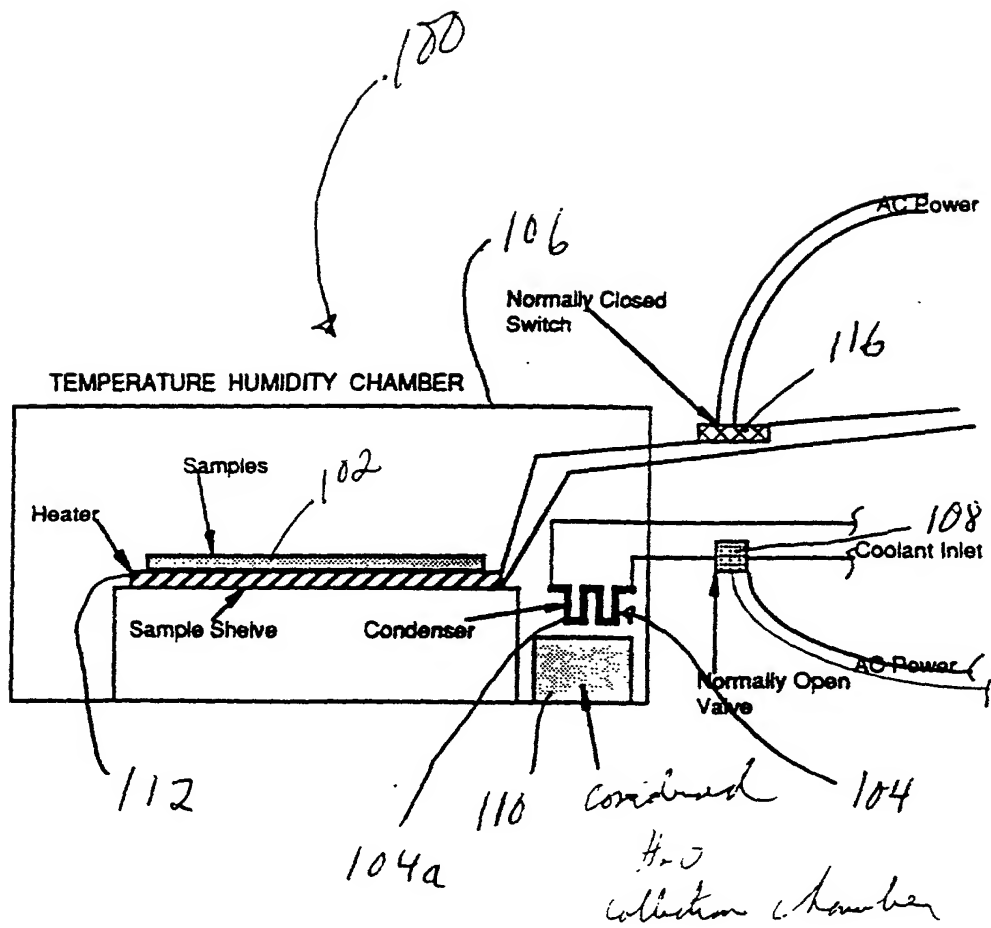


Fig 22

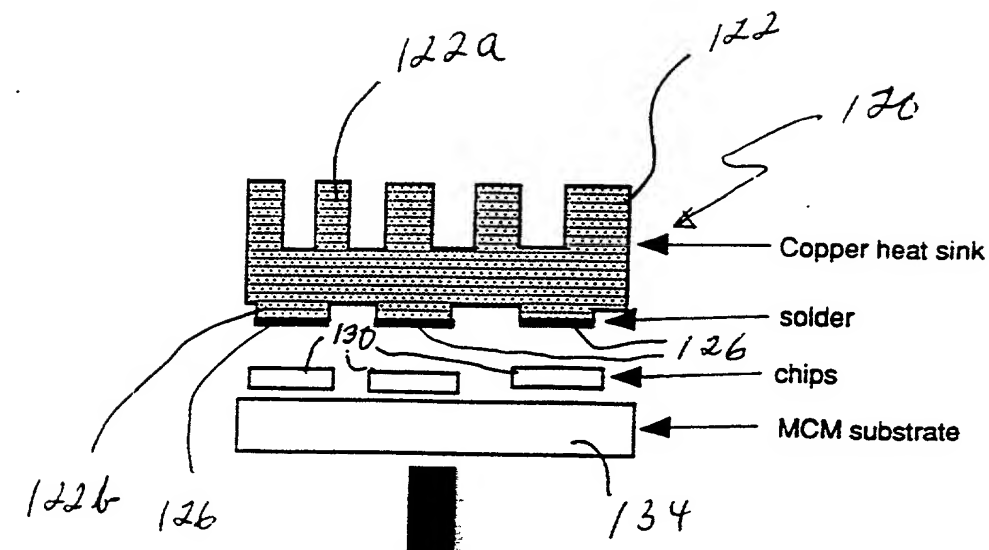
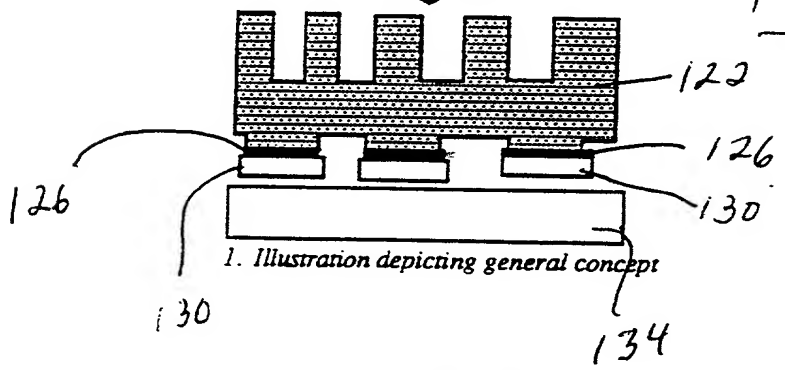
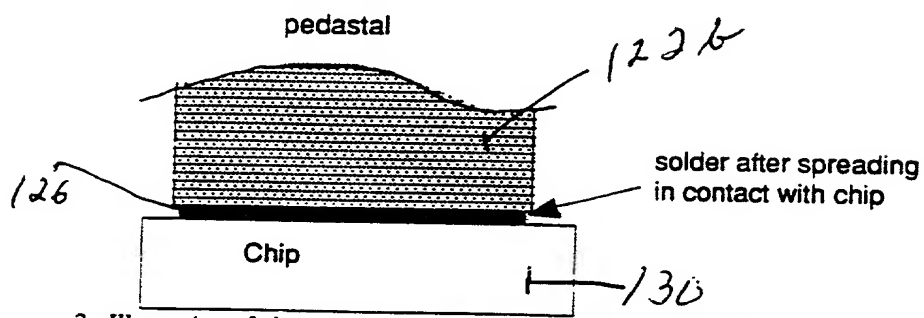


Fig. 23



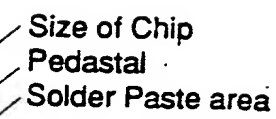
1. Illustration depicting general concept



2. Illustration of close view of solder pedestal in contact with chip

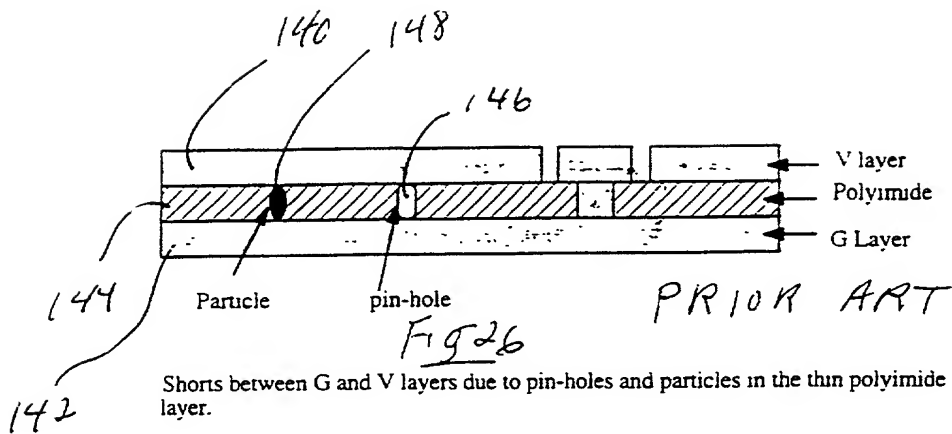
Fig 24

126



130

3. Illustration of top view of pedastal



#### The New Process

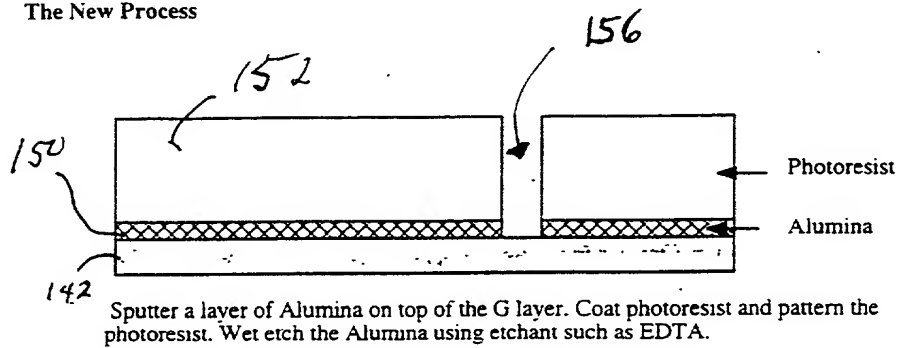


Fig 27

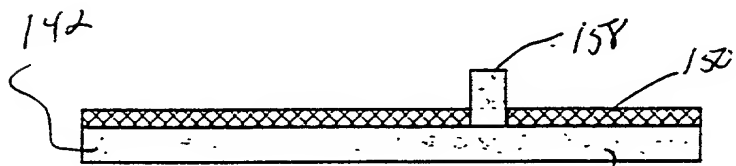
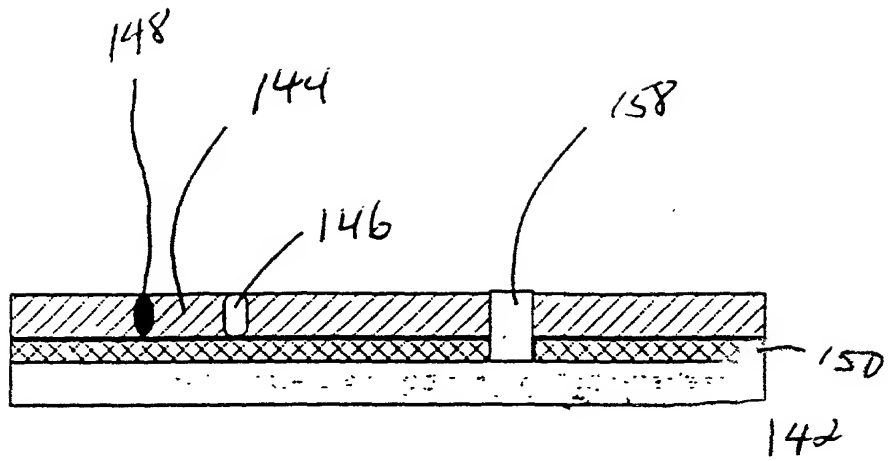


Plate the via and Strip the photoresist.

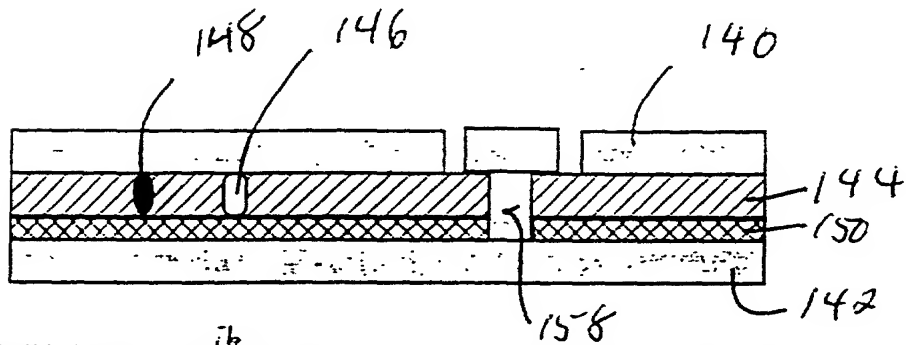
Fig 28

201602-55495001



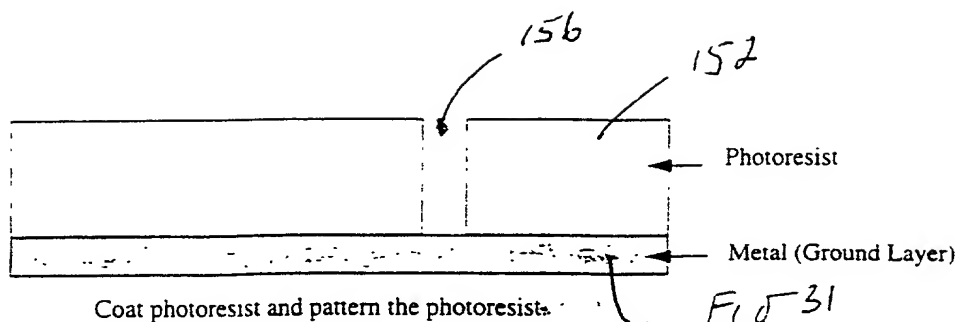
Coat polyimide, and then planarize and expose the vias.

Fig 29



Build V layer. Even there are pin-holes and particles in the polyimide layer, no shorts occur between G and V layers.

Fig 30



Coat photoresist and pattern the photoresist.

142 Fig 31

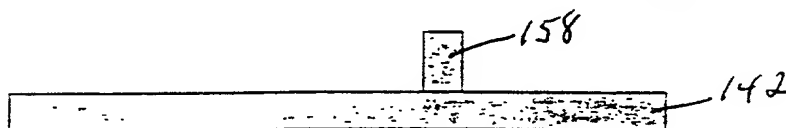
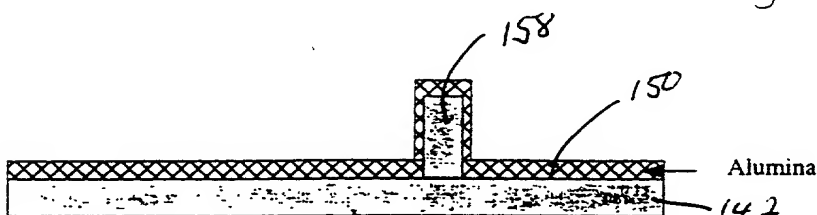


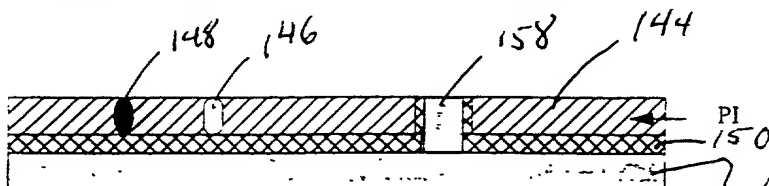
plate vias, strip resist, and etch seed (if needed)

Fig 32



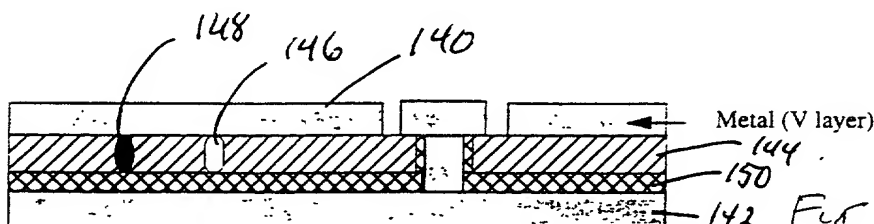
Deposit alumina (or other type of dielectric materials). Deposition processes include CVD, PVD, or sol-gel process.

Fig 33



Coat PI layer and then planarize and expose the vias

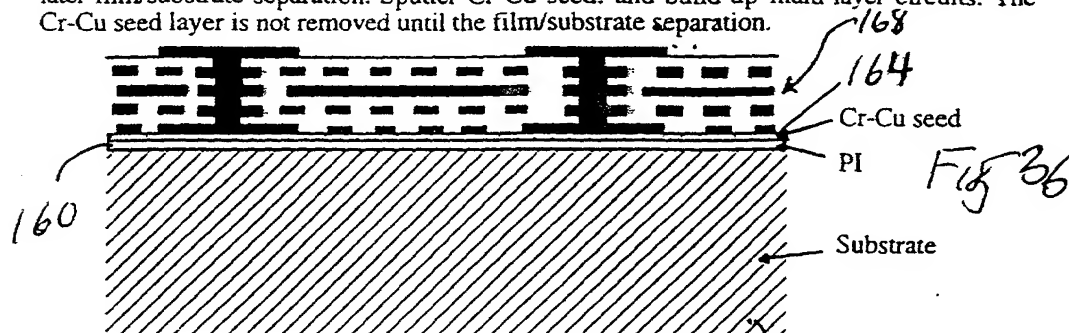
Fig 34  
142



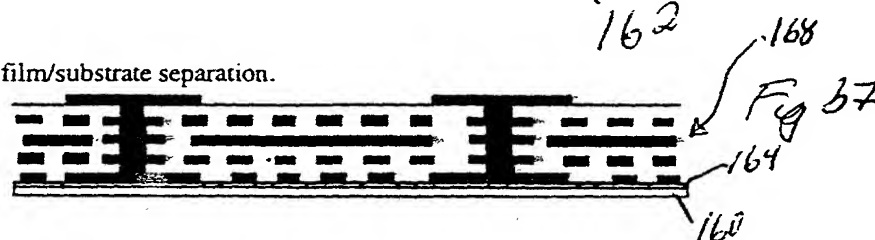
Build V layer. Even there are pinholes and particles in the polyimide layer, no shorts occur between G and V layers.

-142 Fig 35

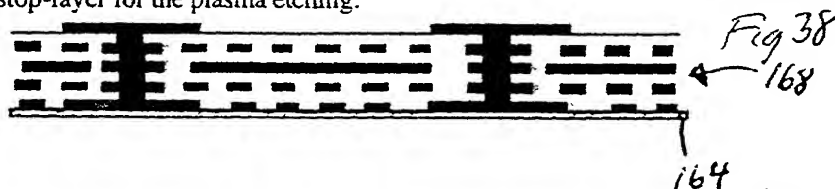
Coat a polyimide layer on top of a substrate. The substrate may be pre-treated for later film/substrate separation. Sputter Cr-Cu seed, and build up multi-layer circuits. The Cr-Cu seed layer is not removed until the film/substrate separation.



After film/substrate separation.



The polyimide layer is etched away using oxygen plasma. The Cr-Cu seed layer serves as the stop-layer for the plasma etching.



After wet etch of Cr-Cu seed.



Fig 39

1055436 020102



Fig. 40 Coat a polyimide layer on top of a substrate and sputter Cr-Cu seed on top of the polyimide. The substrate may be pre-treatment for later film/substrate separation. The seed is etched away after completing the first metal pattern layer. Multi-layer circuits are then built.

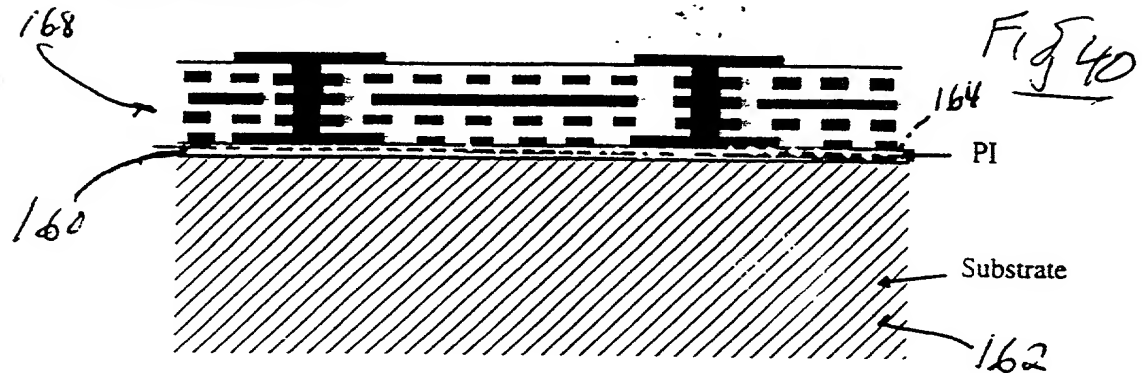


Fig. 41 After film/substrate separation

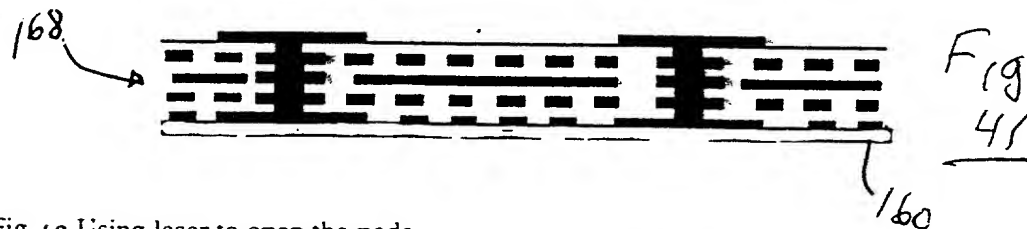
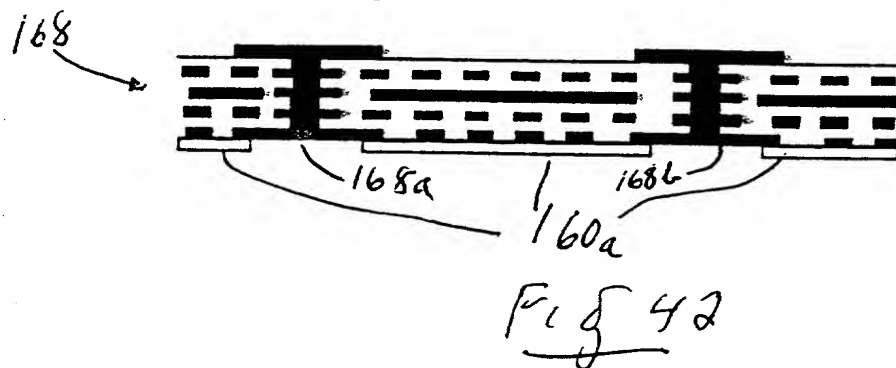


Fig. 42 Using laser to open the pads



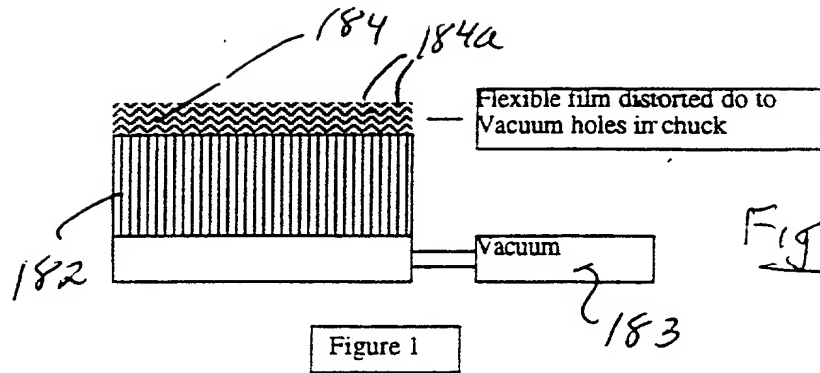


Fig 43

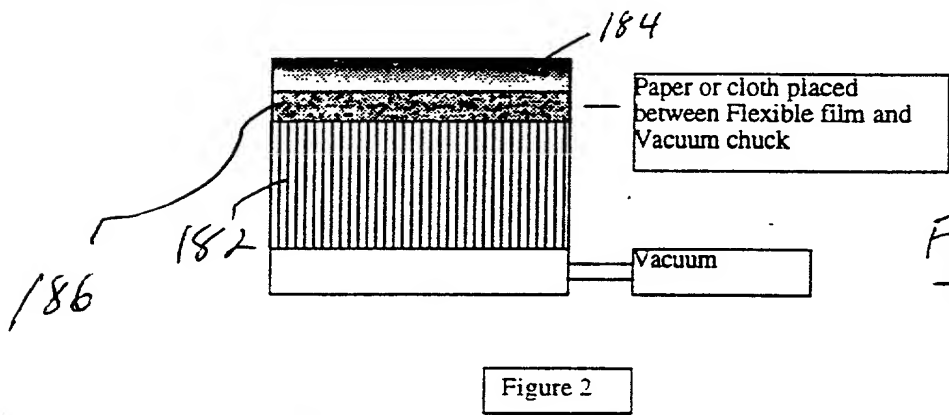


Fig 44

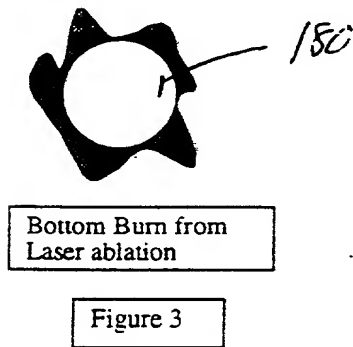


Fig45

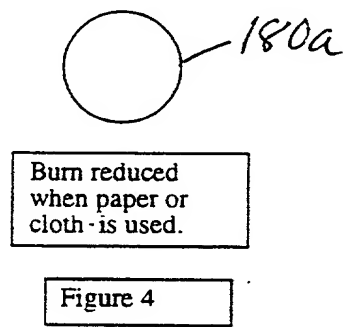
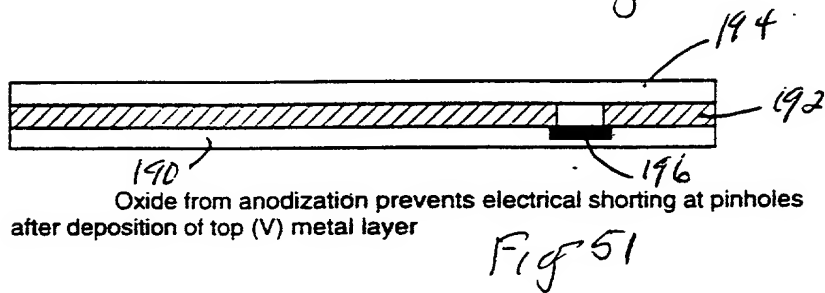
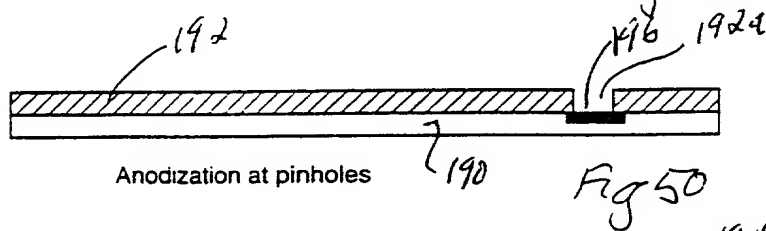
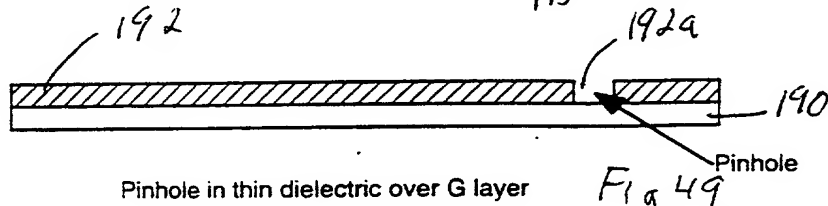
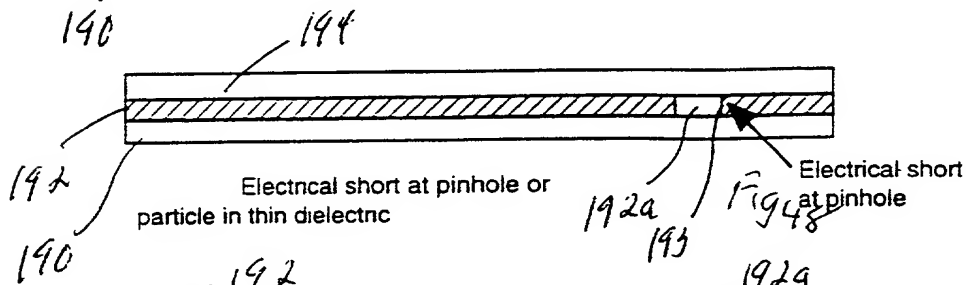
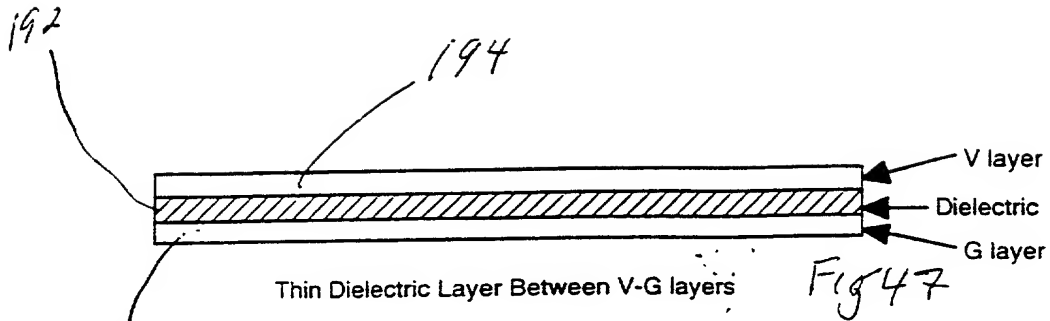


Fig46



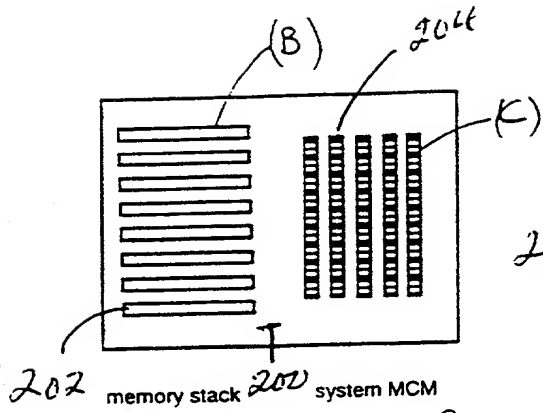


Fig 52A

Case (I)

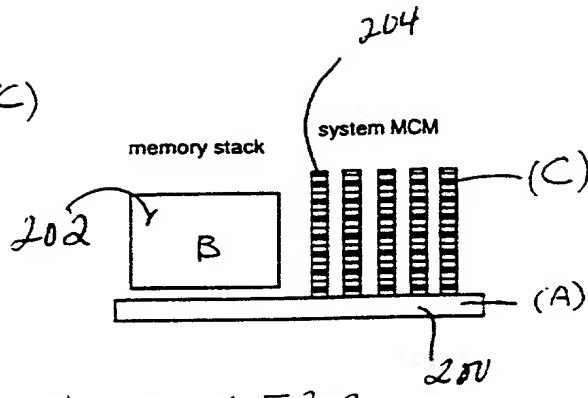


Fig 52B

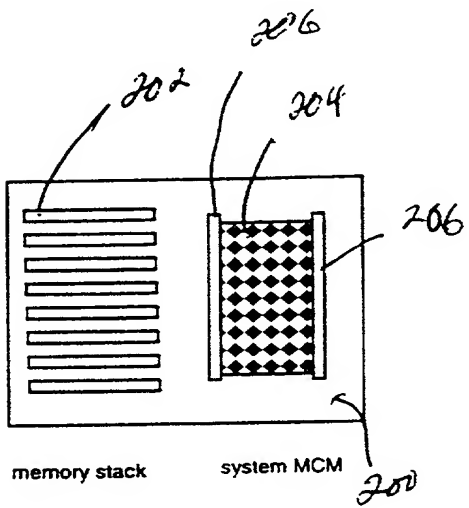


Fig 53A

Case (II)

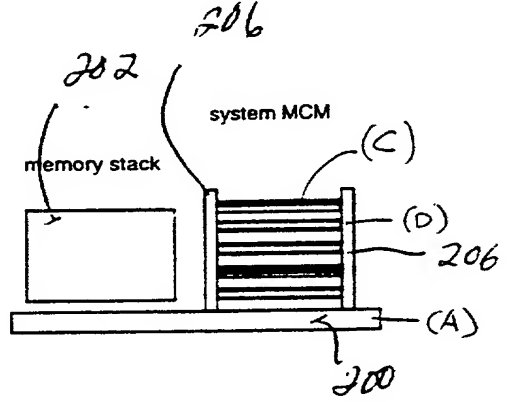
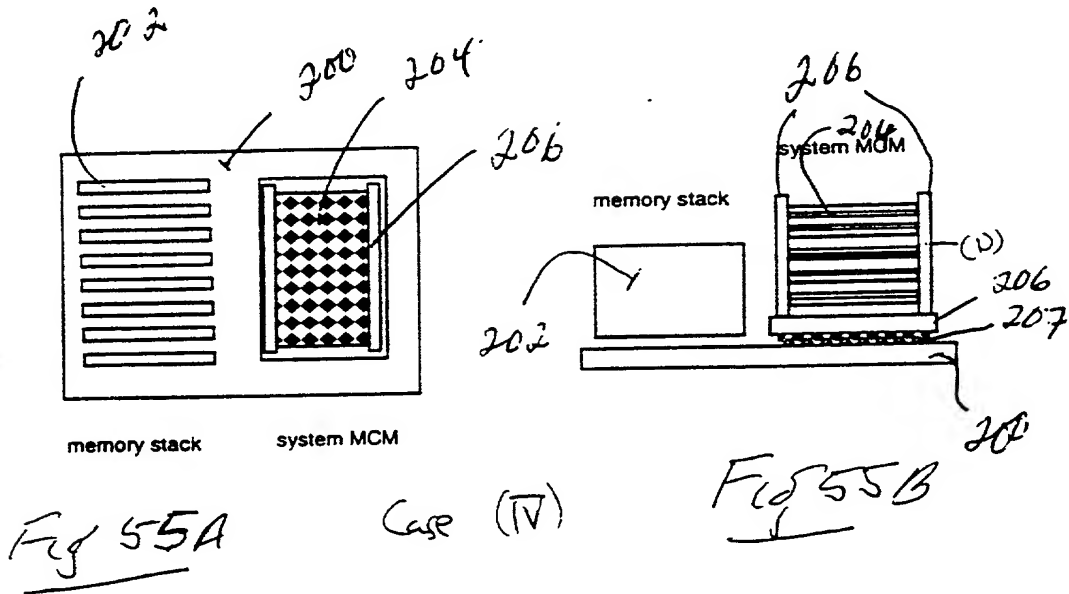
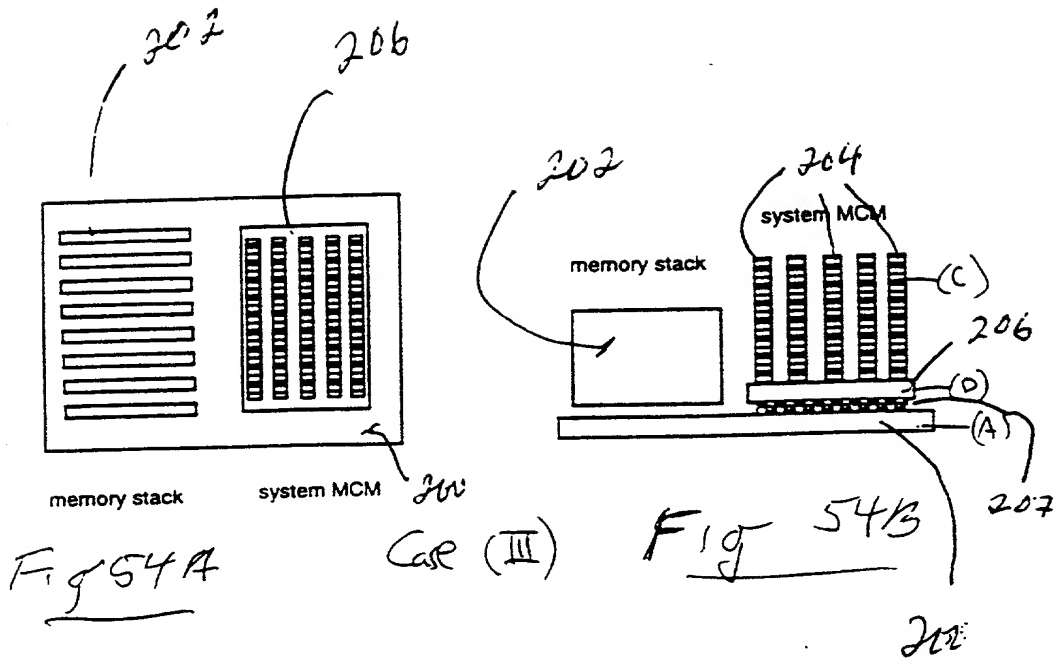


Fig 53B

2010055459001



10064936 020707

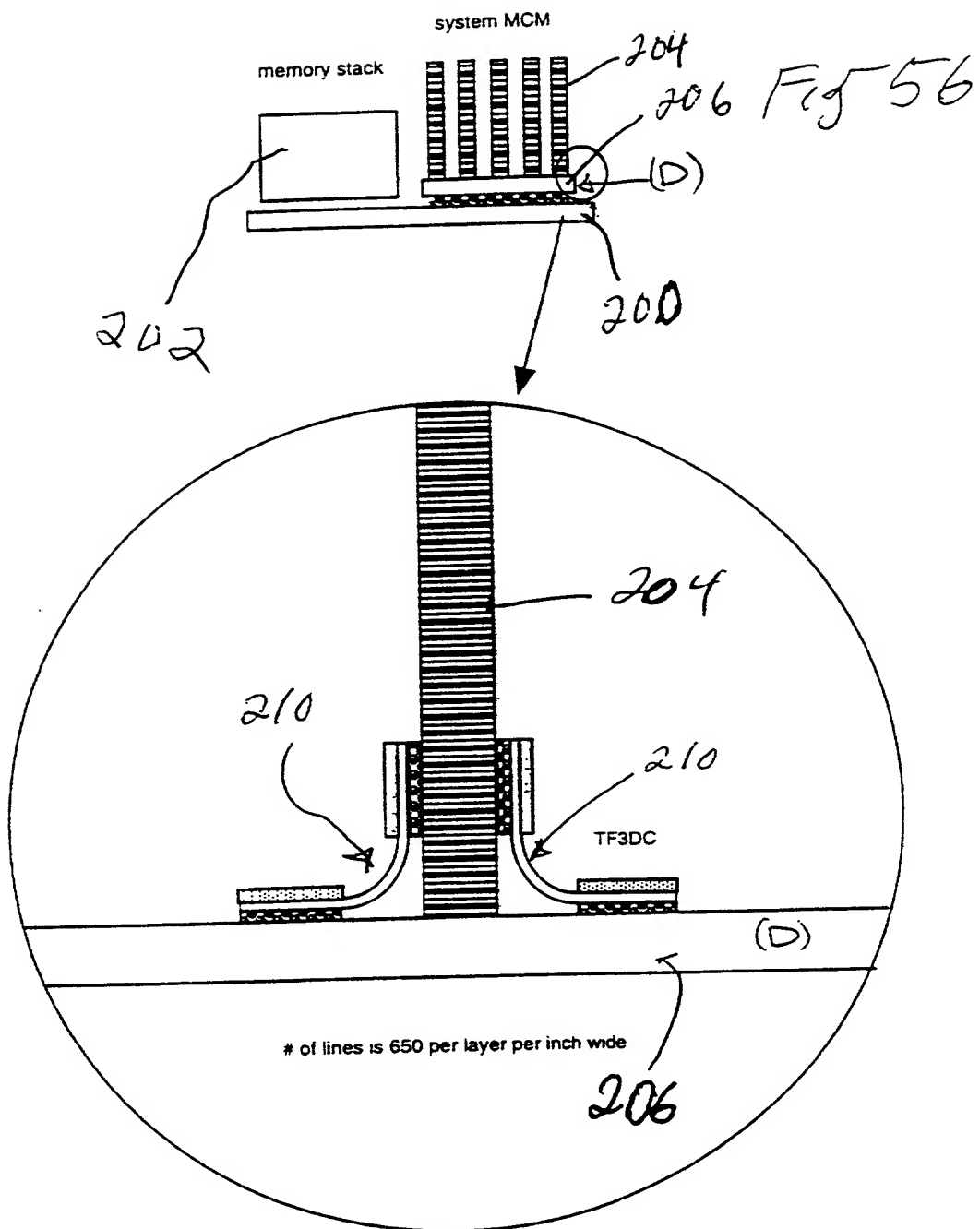


Fig 57

1006495-020103

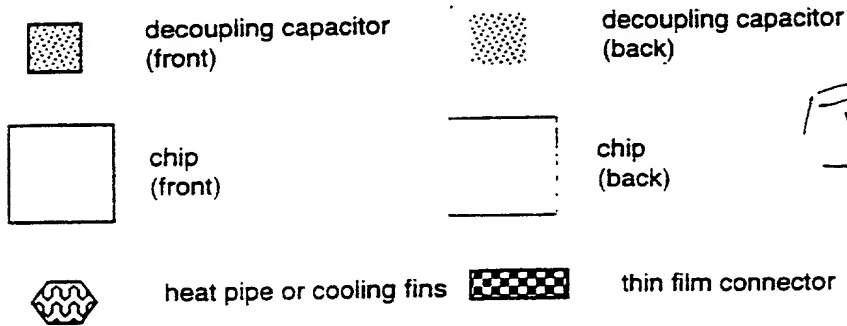
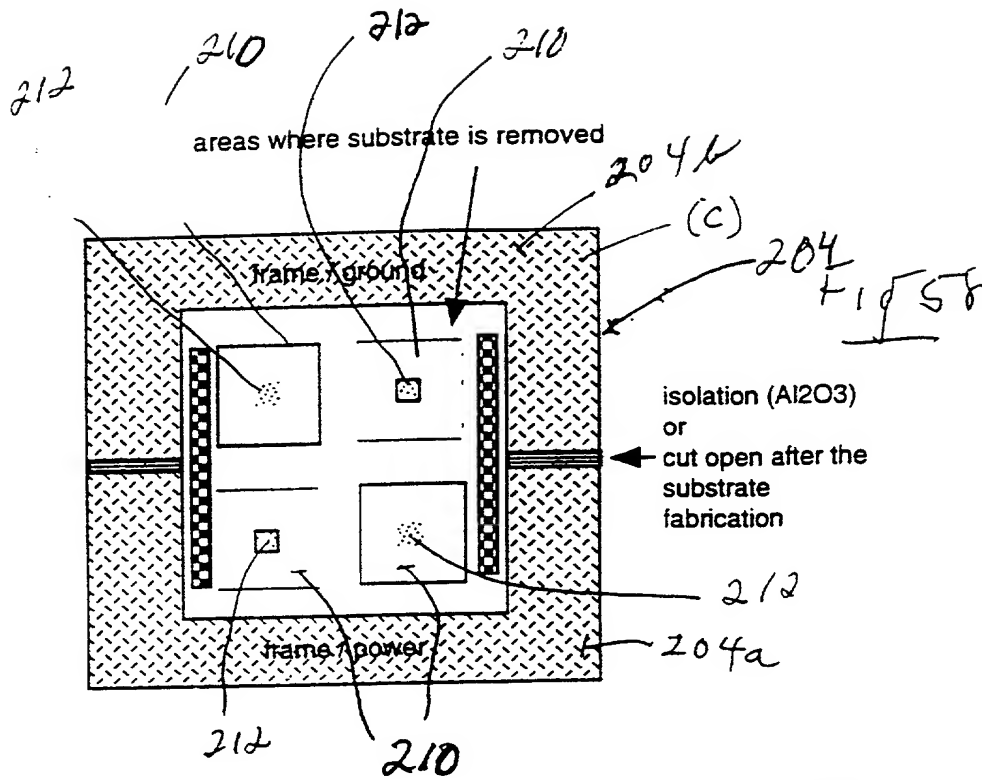


Fig 59

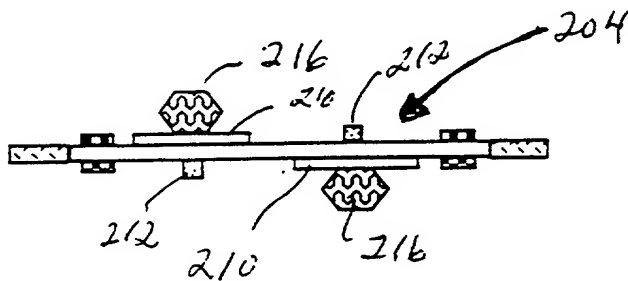
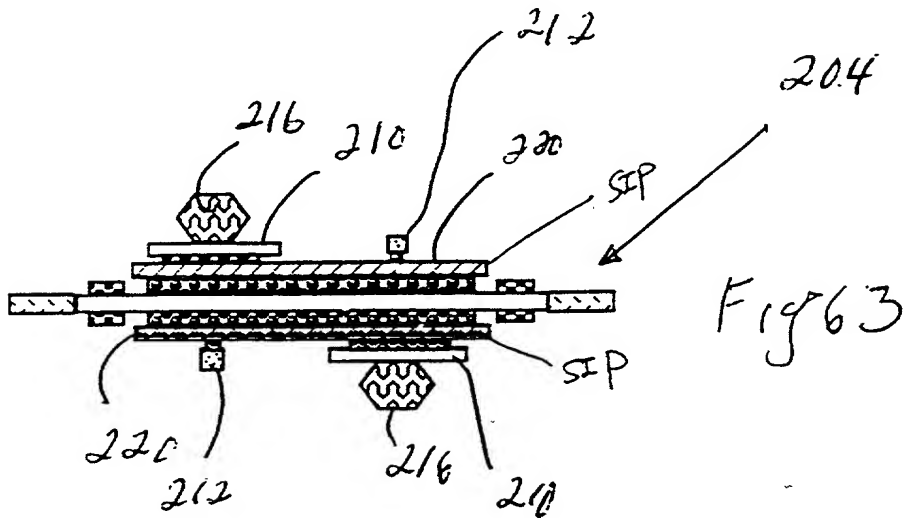
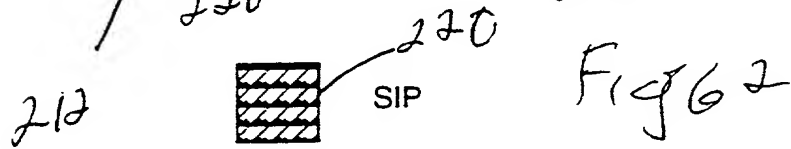
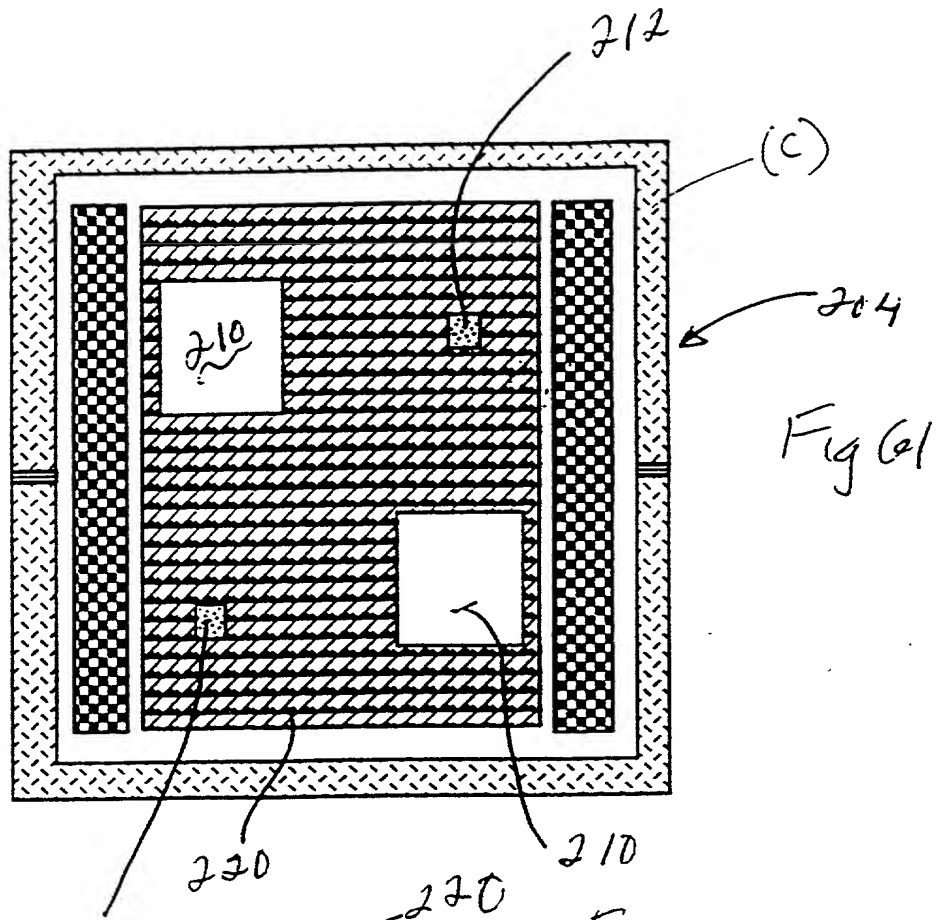


Fig 60





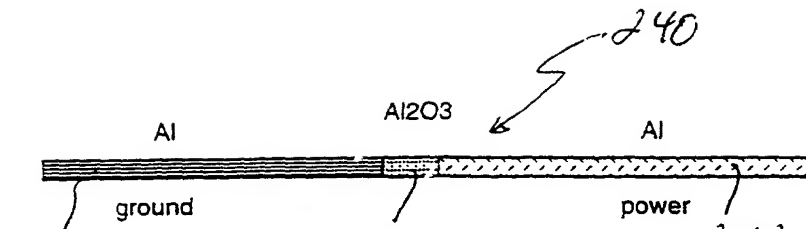


Fig 64

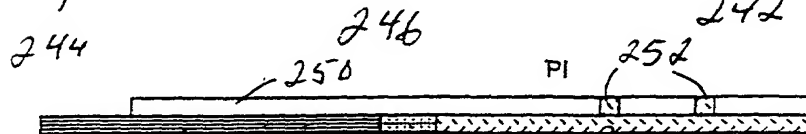


Fig 65

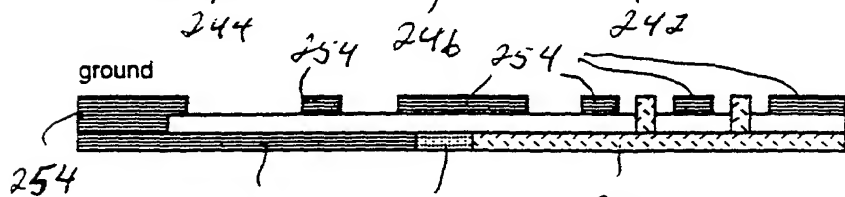


Fig 66

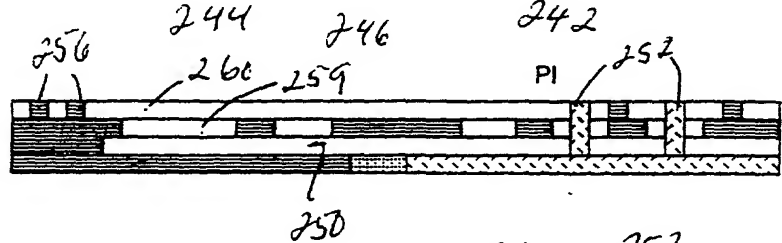


Fig 67

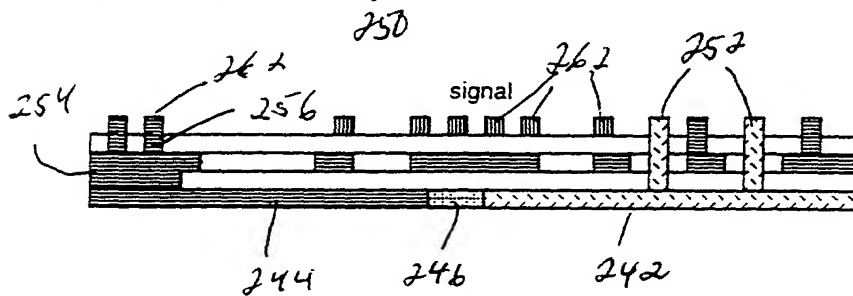


Fig 68

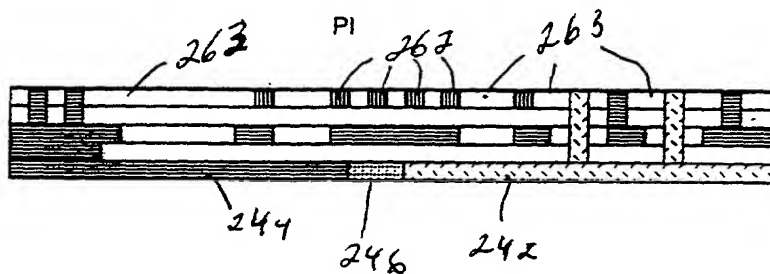


Fig 69

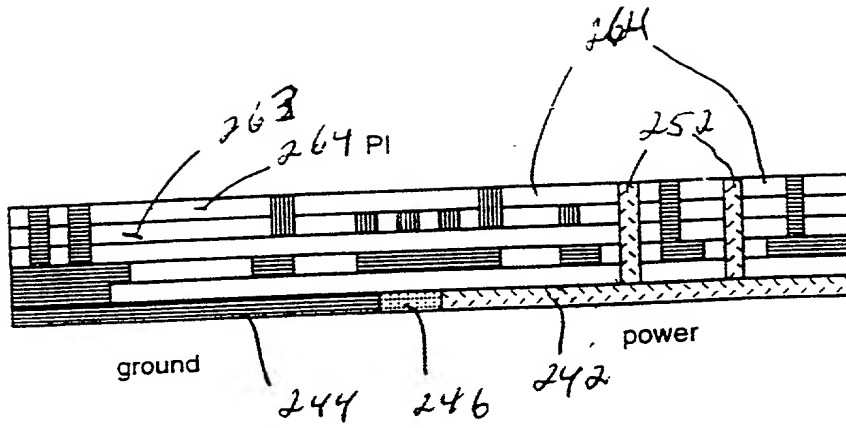


Fig 70

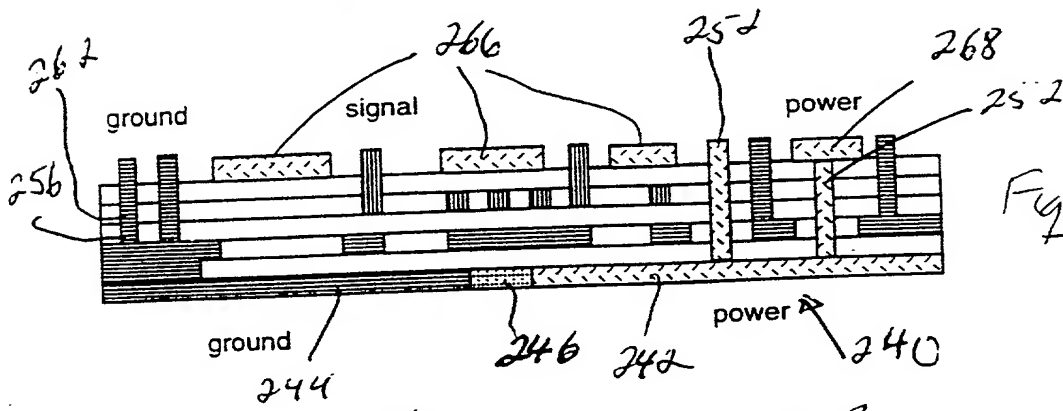


Fig 71

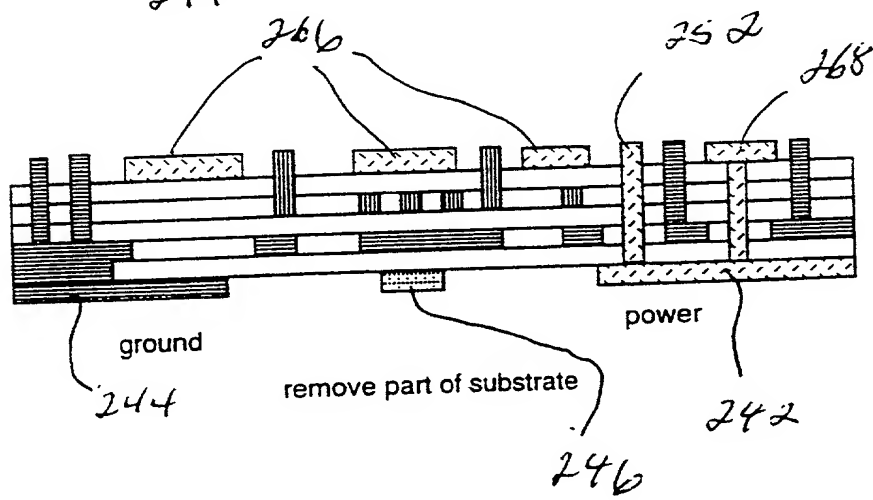


Fig 72

1005495-00403

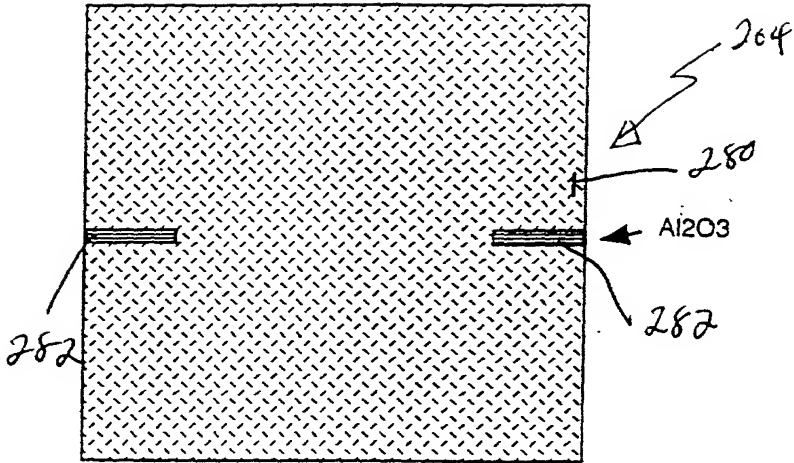


Fig. 73

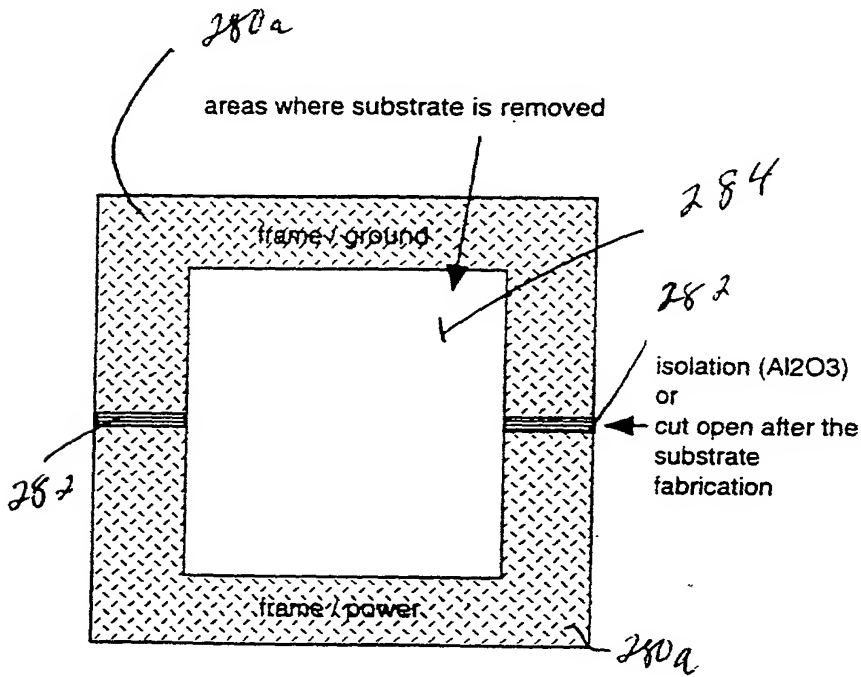


Fig. 74

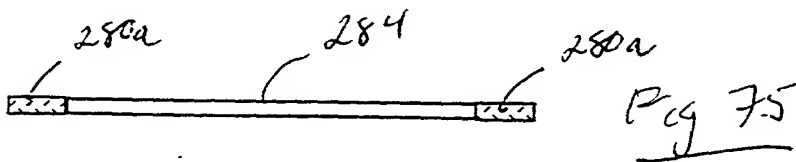


Fig. 75

Traditional process for anisotropic conductive film (ACF) connection process for joining two substrate.

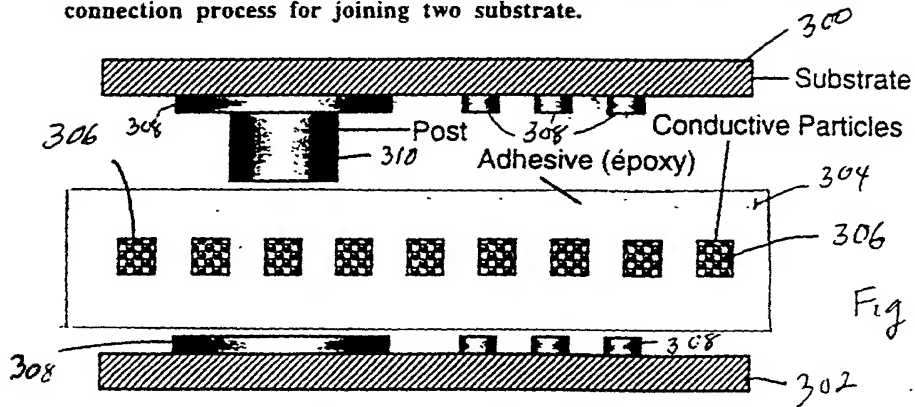


Fig. 76

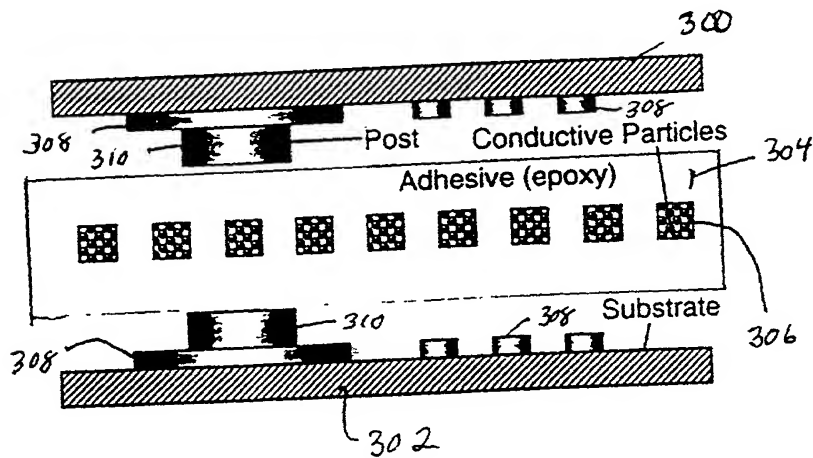


Fig 77

ACF connection after lamination under high pressure and high temperature in traditional ACF process

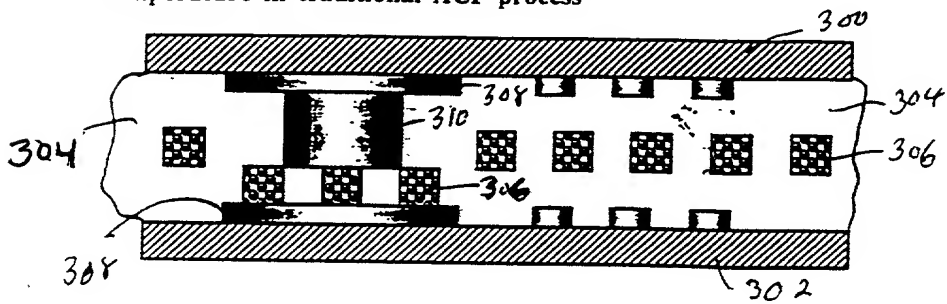


Fig 78

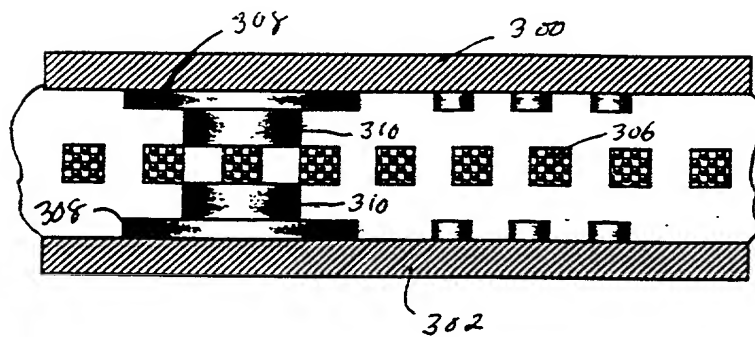
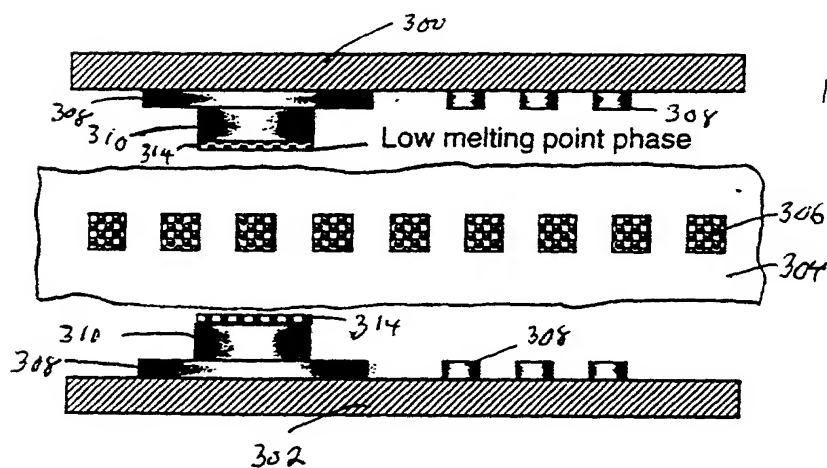
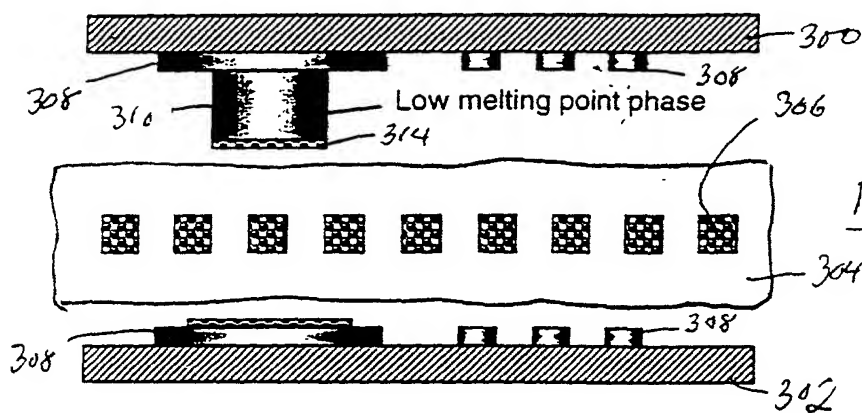


Fig 79

Low resistance ACF joints by depositing a thin layer of low-melting-point metal that will form intermetallic compound/alloy between post material and conductive particles in ACF.



After joining process (high pressure and high temperature), intermetallic/alloy formed at the interface of post and conductive particles. The intermetallic/alloy will decrease the contact resistance from traditional ACF process and provide a stronger mechanical bond.

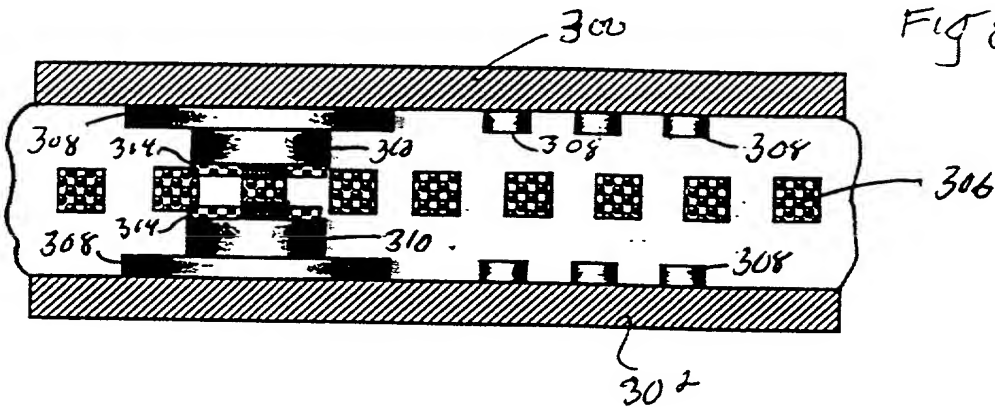
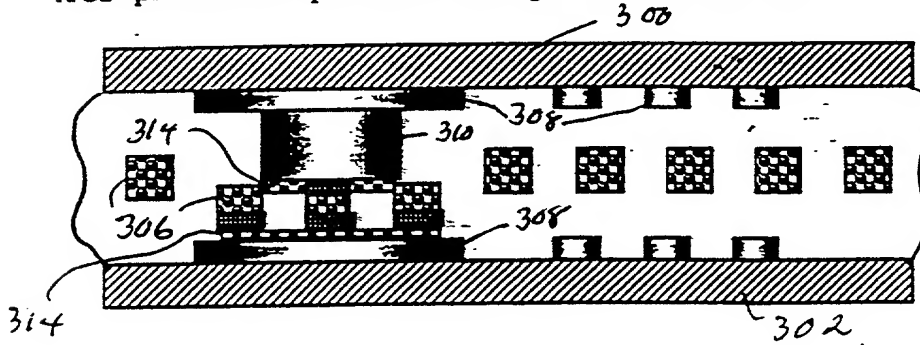
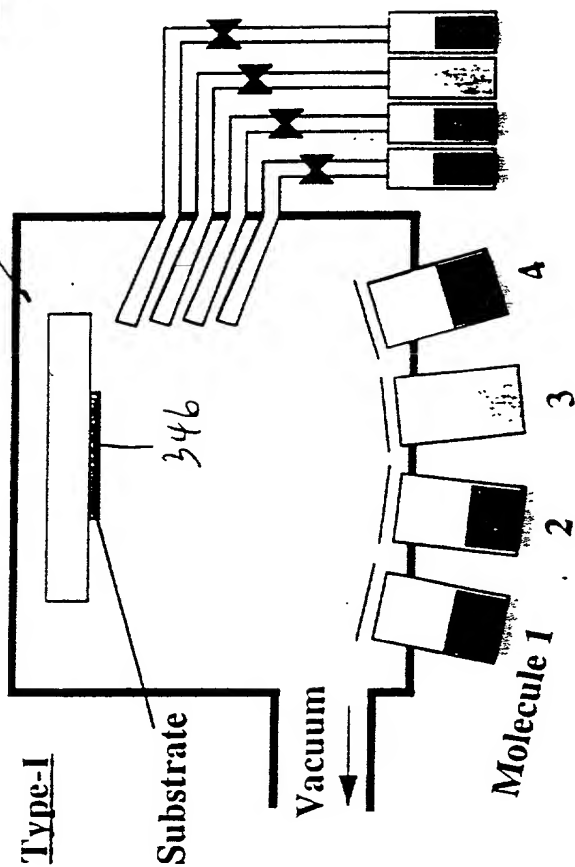






Fig. 85A



Type-I

Substrate

Molecule 1

Type-II

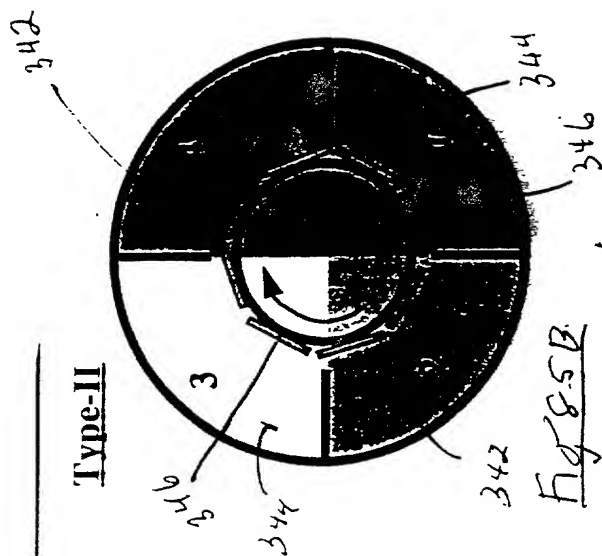


Fig. 85B

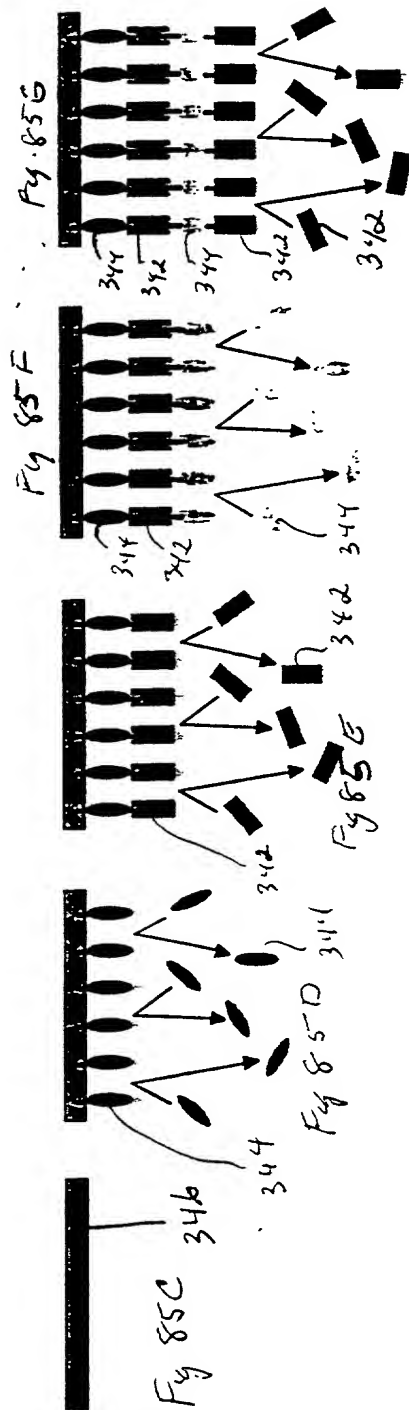


Fig 85C

Fig 85D

Fig 85E

Fig 85F

## Vapor Phase Deposition Vs. Spin coating

	Spin coating		Vapor Phase Deposition	
			CVD	MLD
-Coverage Controllability	Low		High	High
-Thickness Accuracy/Uniformity	Low		Medium	High
-Deposition Rate	High		Medium	Low
-Molecular-level Controllability	Low		Medium	High
-Selective Deposition	No		Yes	Yes
Selective Molecular Alignment	No		Yes	Yes

(High & Yes are preferable)

-Conformable coverage and Thickness accuracy/uniformity

-CVD/MLD are superior to Spin Coating

- Low  $\epsilon$  insulator with strong adhesion

-MLD may provide high adhesion with the Molecular-Level Controllability

-Options

-CVD/MLD can do # Selective Deposition (hydrophilic/hydrophobic surface)

# Selective Molecular Alignment (surface treatment)

may provide further  $\epsilon$  reduction, process simplification, and low Cu-diffusion

Fig 85H



**PMDA**

**ODA**

naphthalene dianhydride (ND)

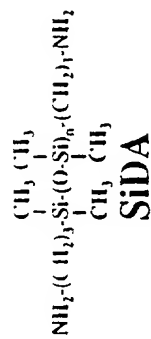
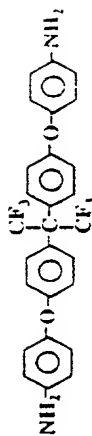
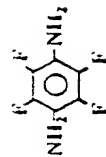
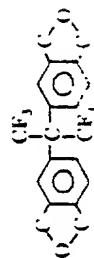


Fig. 86.CC

# SIDA



# Bis-OAF



**VT4-1A**

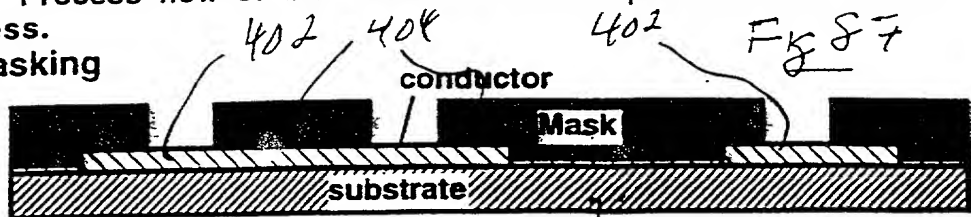
alkylamine-coated Si | ND ⇌ Bis-OAF ⇌ ND ⇌ Bis-OAF ⇌ ••• ⇌ ND ⇌ SiDA

Si SIDA ⇨ 6FDA ⇨ Bis-OAI + 6FDA ⇨ SiDA

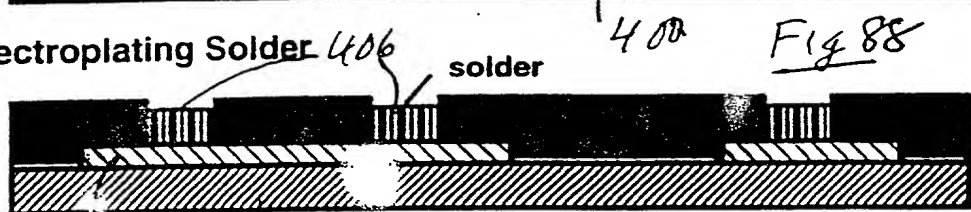
Si

Process flow of the resist-free electroplated solder reflow process.

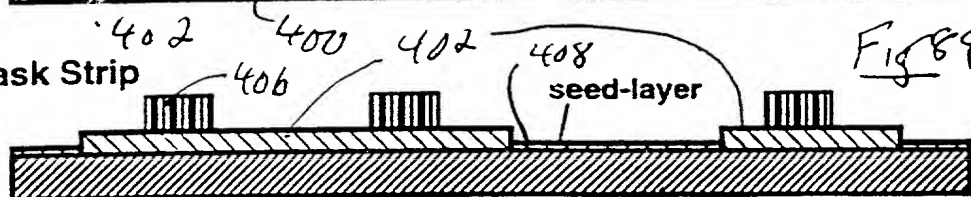
1. Masking



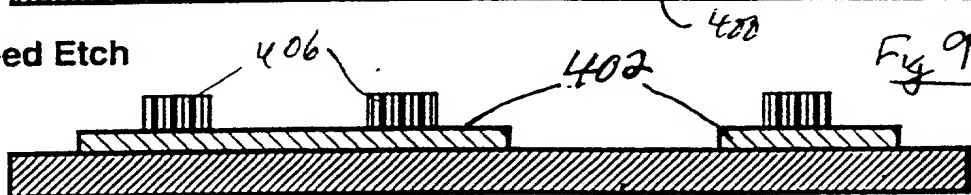
2. Electroplating Solder



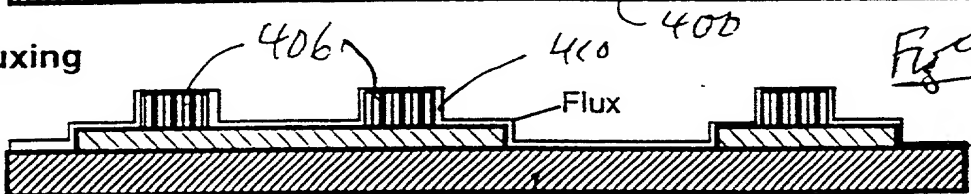
3. Mask Strip



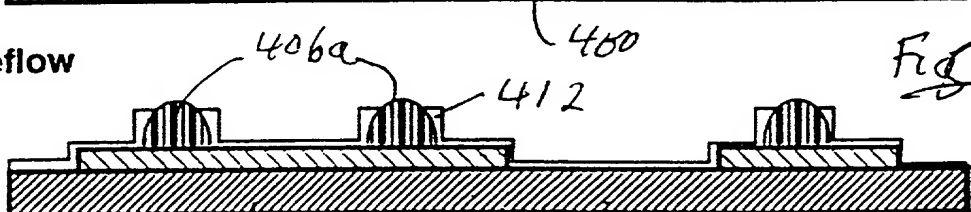
4. Seed Etch



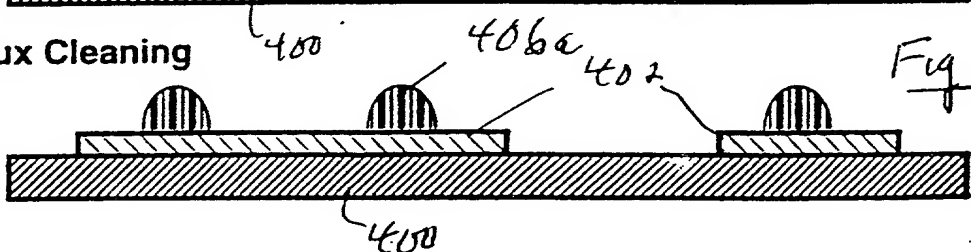
5. Fluxing



6. Reflow

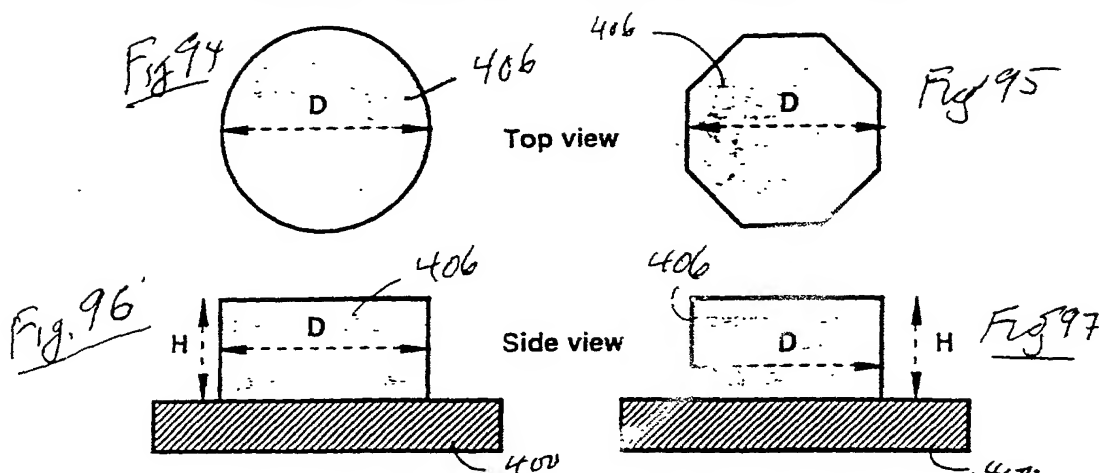


7. Flux Cleaning

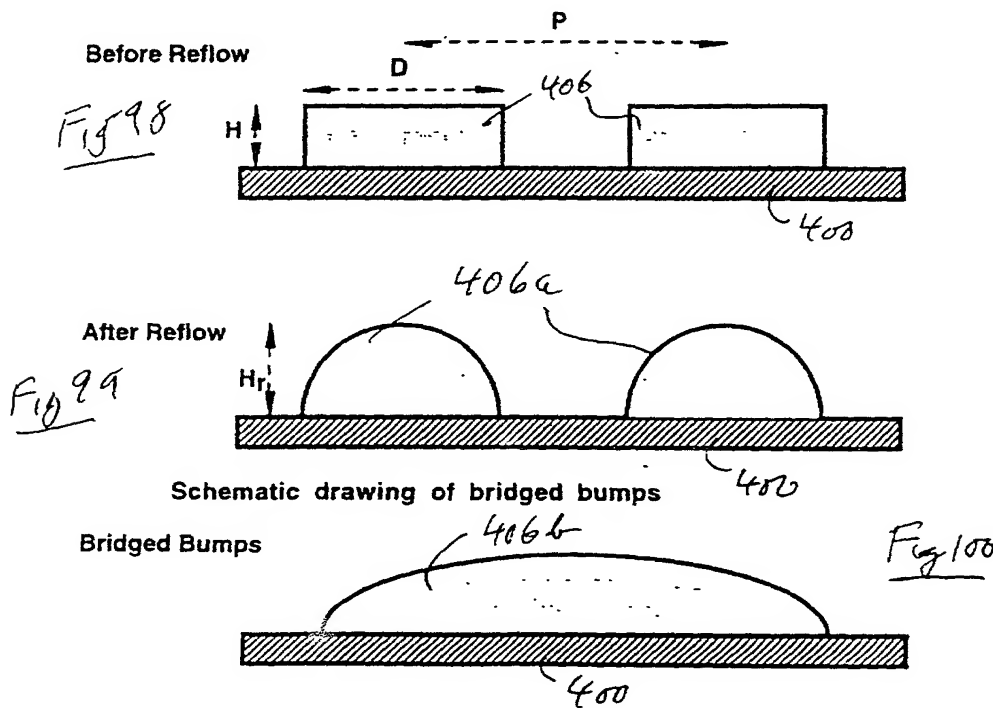


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Geometric dimensions of the electroplated bumps.



Geometric shape change of electroplated solder bumps by reflow process



## Direct Plating Process

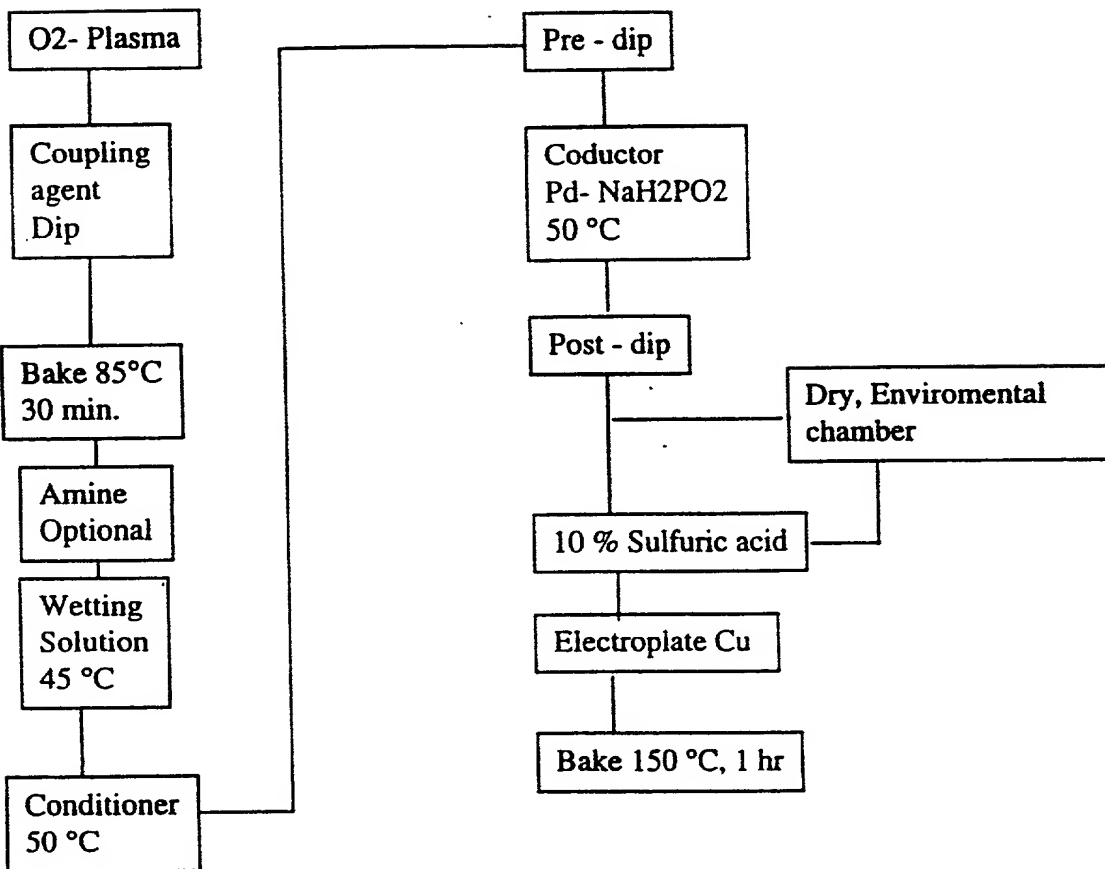


Fig 101A

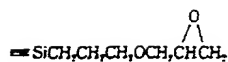
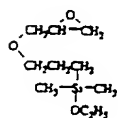
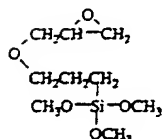


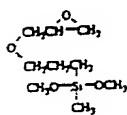
Fig 101B



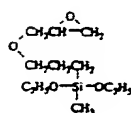
(3-GLYCIDOXYPROPYL)DIMETHYLETHOXY-SILANE  
C<sub>10</sub>H<sub>22</sub>O<sub>3</sub>Si



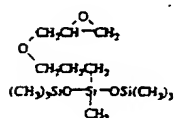
(3-GLYCIDOXYPROPYL)TRIMETHOXY-SILANE  
3-(2,3-EPOXYPROPOXY)PROPYLTRIMETHOXY-SILANE  
C<sub>9</sub>H<sub>20</sub>O<sub>5</sub>Si



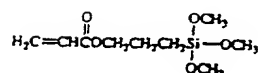
(3-GLYCIDOXYPROPYL)METHYLDIMETHOXY-SILANE  
C<sub>9</sub>H<sub>20</sub>O<sub>4</sub>Si



(3-GLYCIDOXYPROPYL)METHYLDIETHOXY-SILANE  
C<sub>11</sub>H<sub>24</sub>O<sub>4</sub>Si



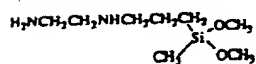
(3-GLYCIDOXYPROPYL)BIS(TRIMETHYL-SILOXY)METHYLSILANE  
C<sub>13</sub>H<sub>32</sub>O<sub>4</sub>Si<sub>3</sub>



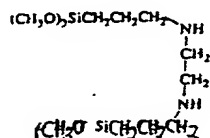
(3-ACRYLOXYPROPYL)TRIMETHOXY-SILANE, 95%  
C<sub>9</sub>H<sub>18</sub>O<sub>5</sub>Si



N-(2-AMINOETHYL)-3-AMINOPROPYLTRI-METHOXY-SILANE  
C<sub>8</sub>H<sub>22</sub>N<sub>2</sub>O<sub>3</sub>Si



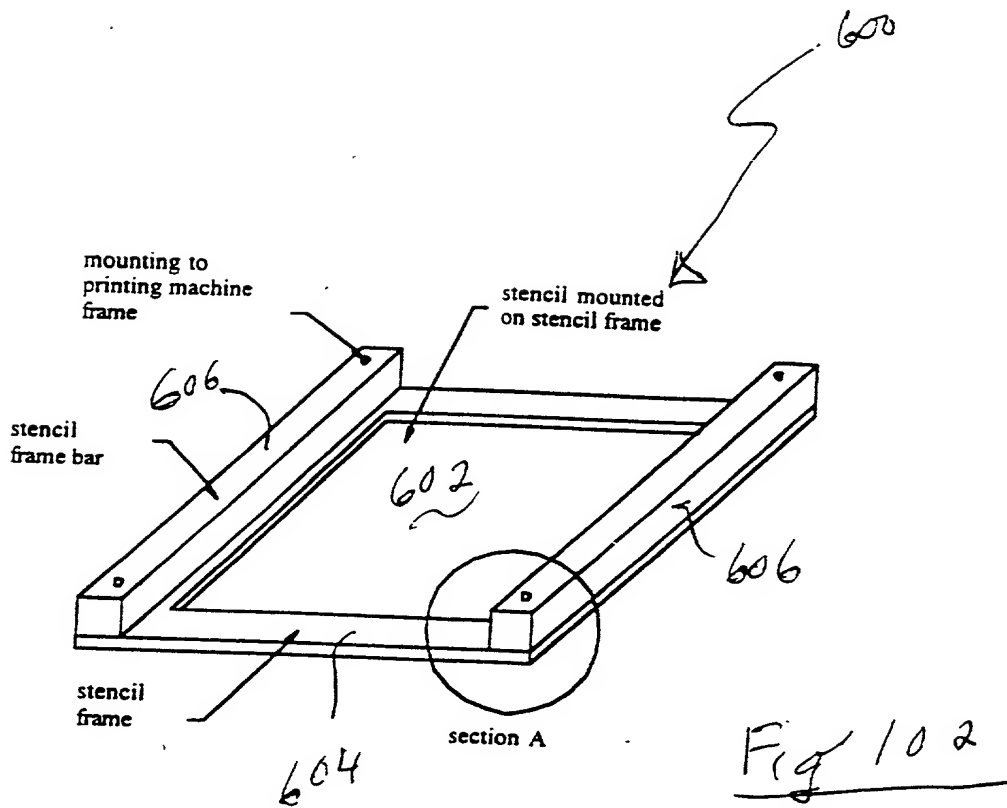
N-(2-AMINOETHYL)-3-AMINOPROPYLMETHYL-DIMETHOXY-SILANE  
C<sub>8</sub>H<sub>22</sub>N<sub>2</sub>O<sub>2</sub>Si



BIS[3-TRIMETHOXY-SILYL]PROPYL-ETHYLENEDIAMINE,  
C<sub>14</sub>H<sub>36</sub>N<sub>2</sub>O<sub>6</sub>Si<sub>2</sub>

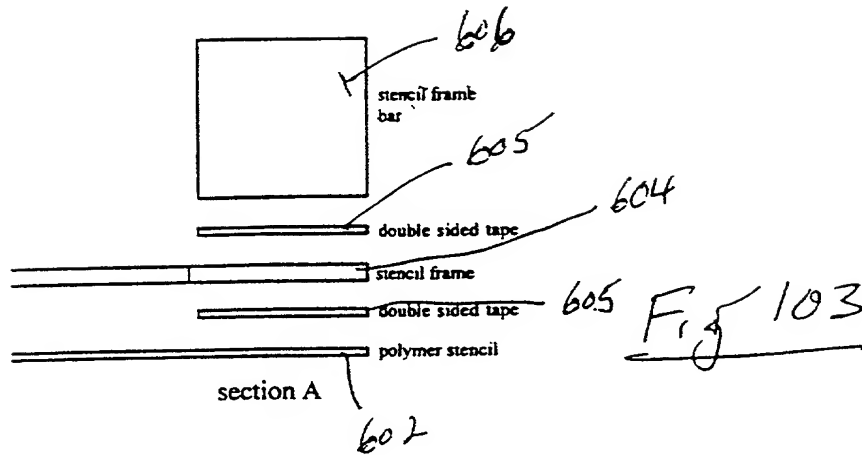


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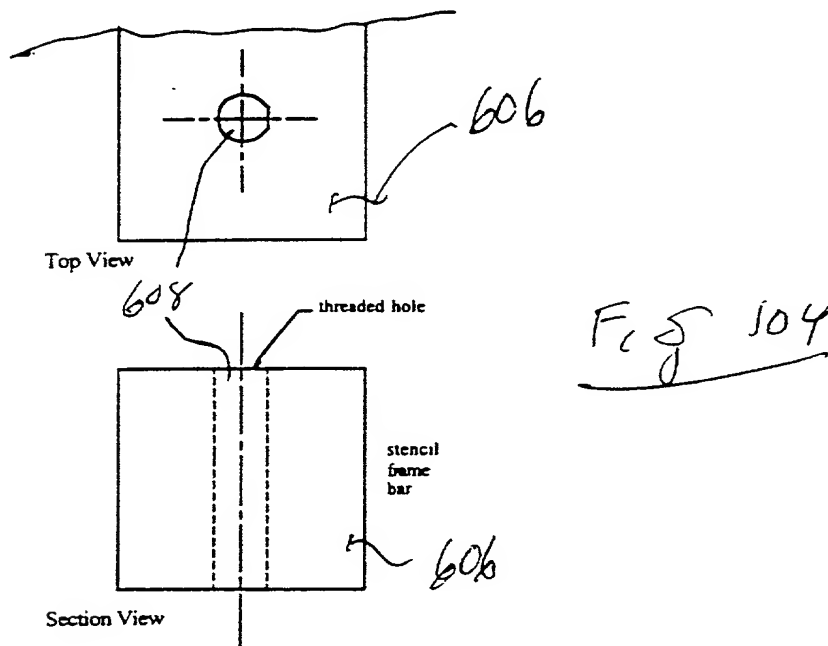


Stencil Frame Layout.

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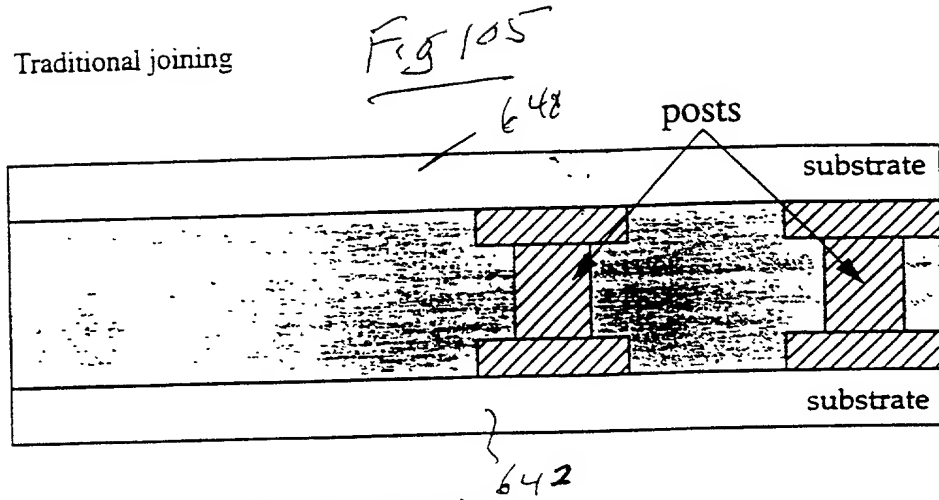


Section View of Stencil Frame Components.

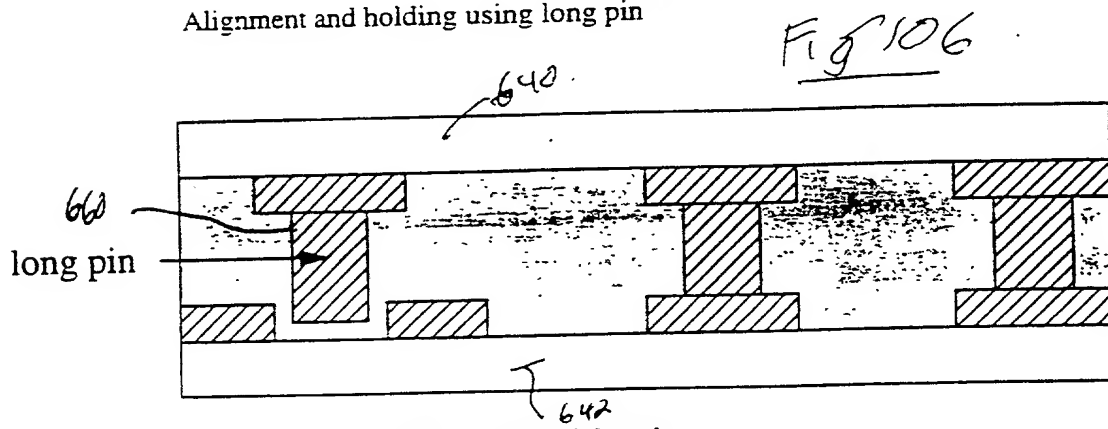


Tapped Hole in Stencil Frame Bar.

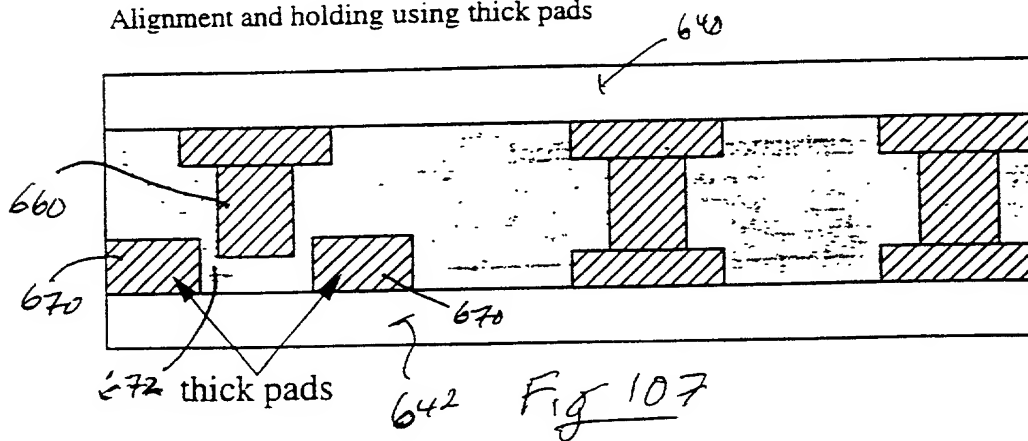
Traditional joining



Alignment and holding using long pin



Alignment and holding using thick pads



Build-up process for long pin

Fig 108

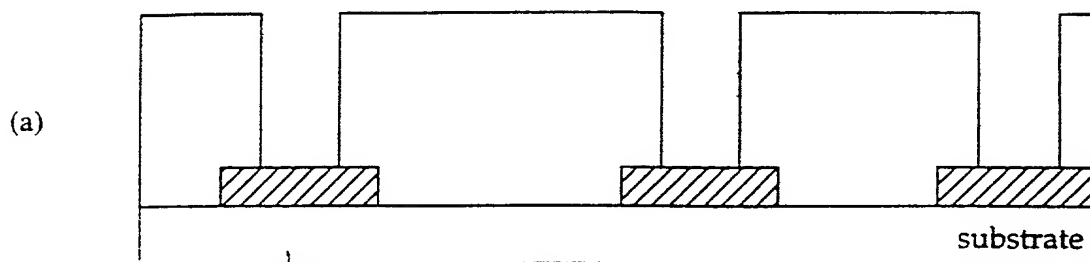
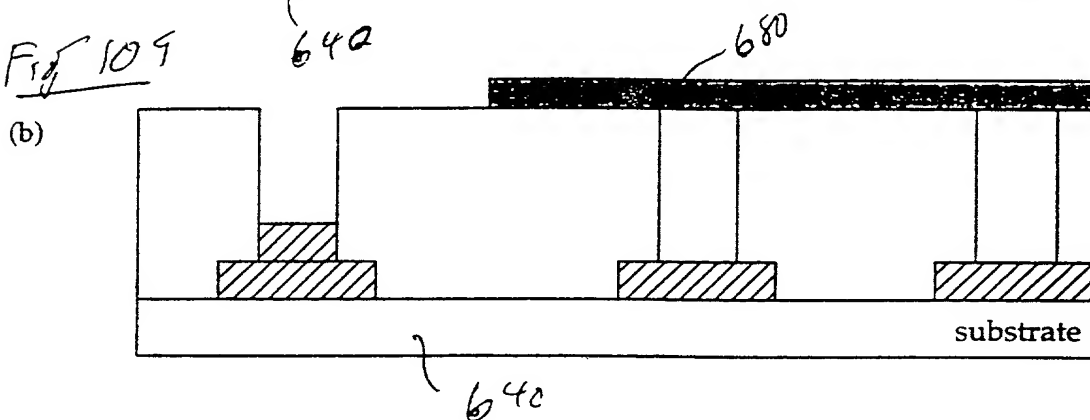


Fig 109



(c)

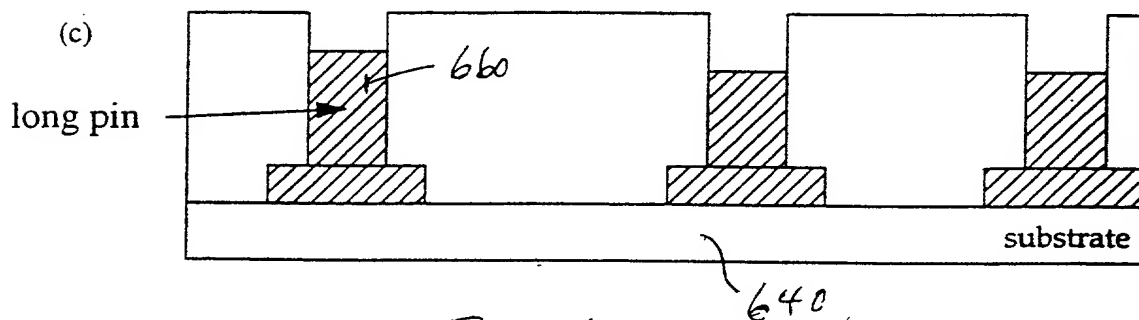


Fig 110

1006456 000100

Fig 111

Another build-up process for long pin

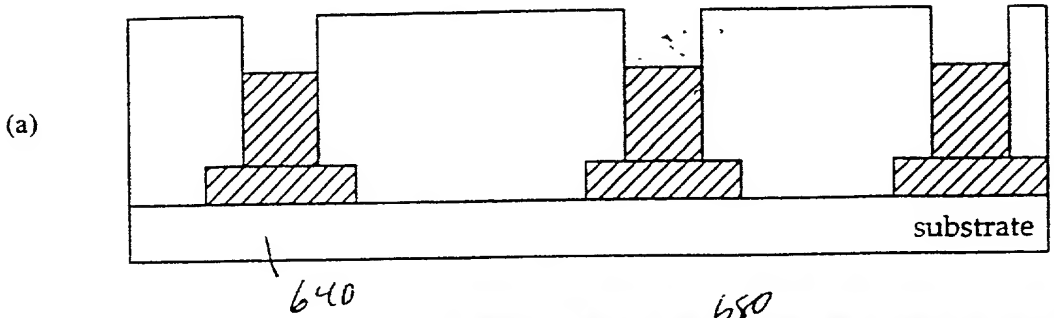


Fig 112

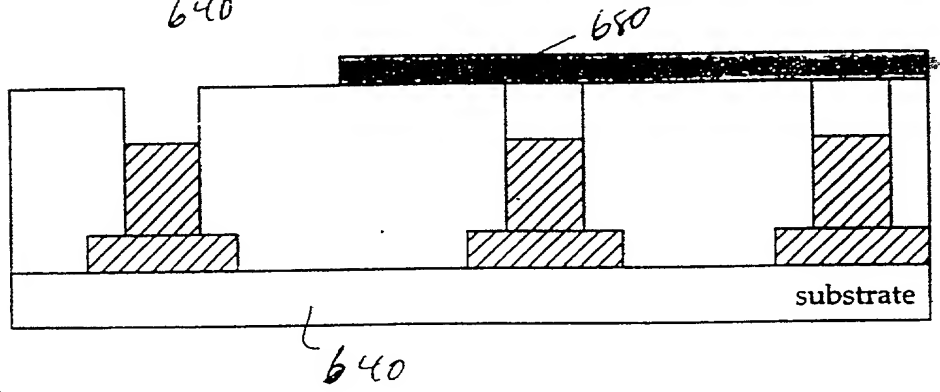
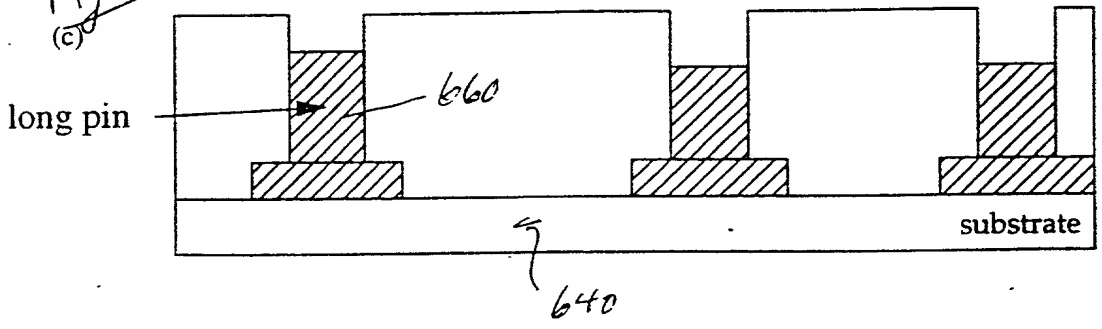


Fig 113



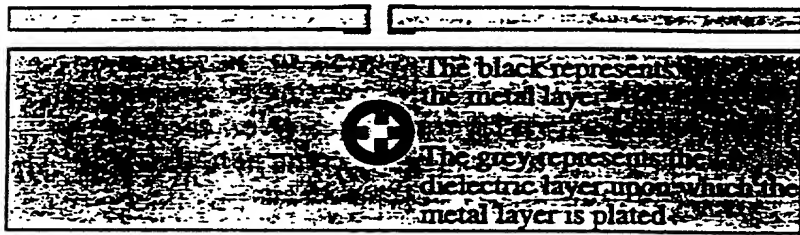
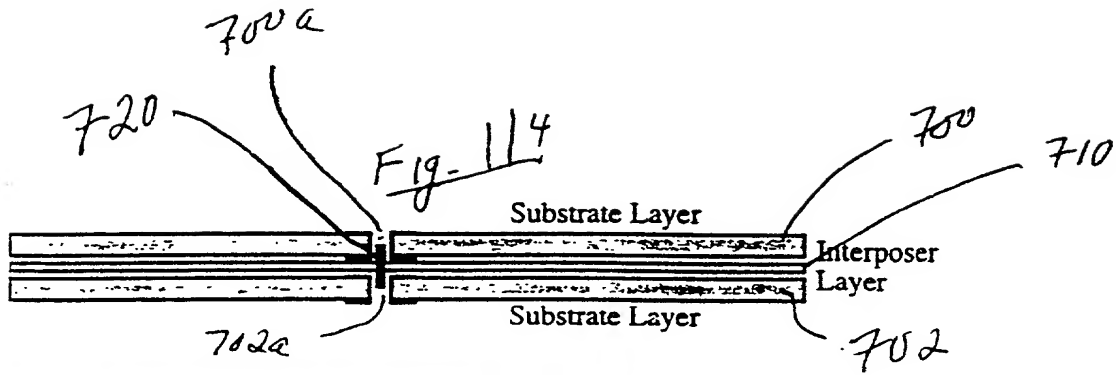


Fig 115

[illegible]

Fig. 11b

Fig. 116

## Transient Liquid Alloy Bonding - Type II

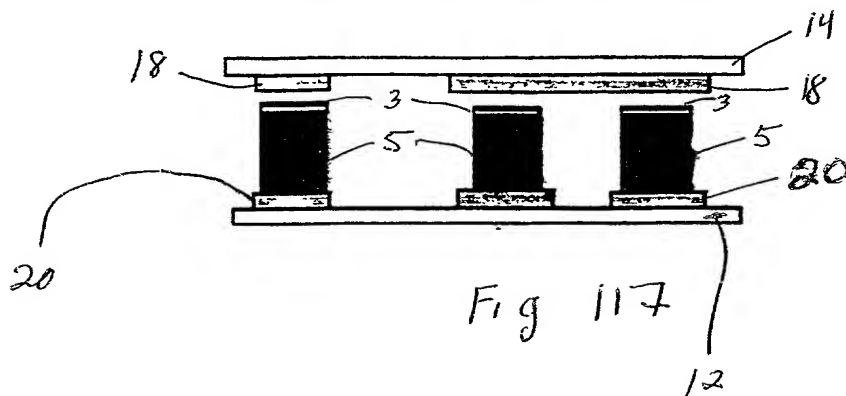
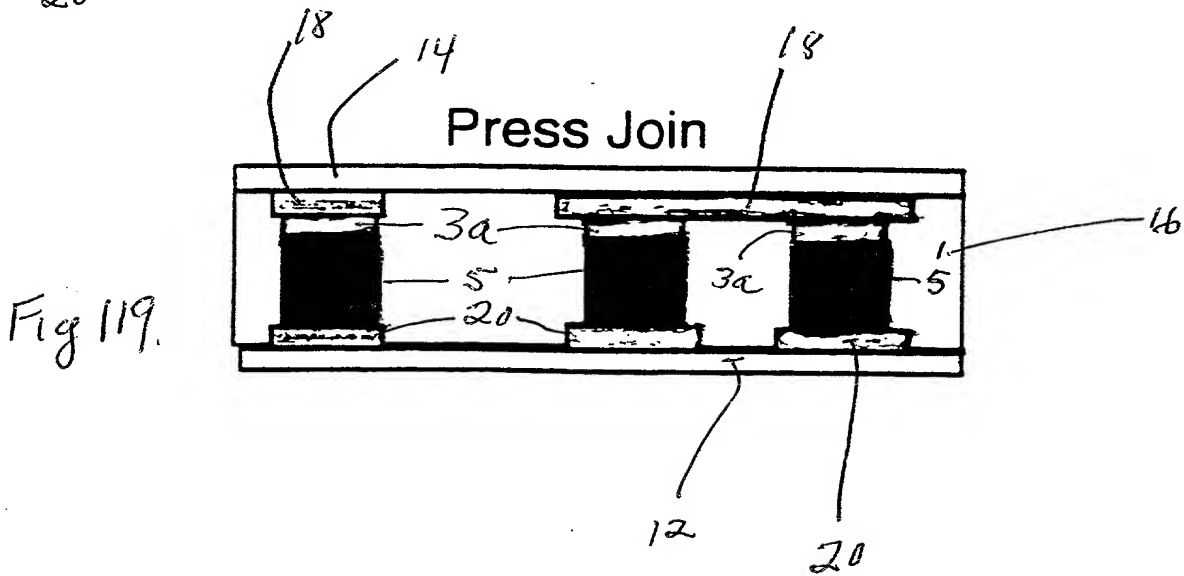
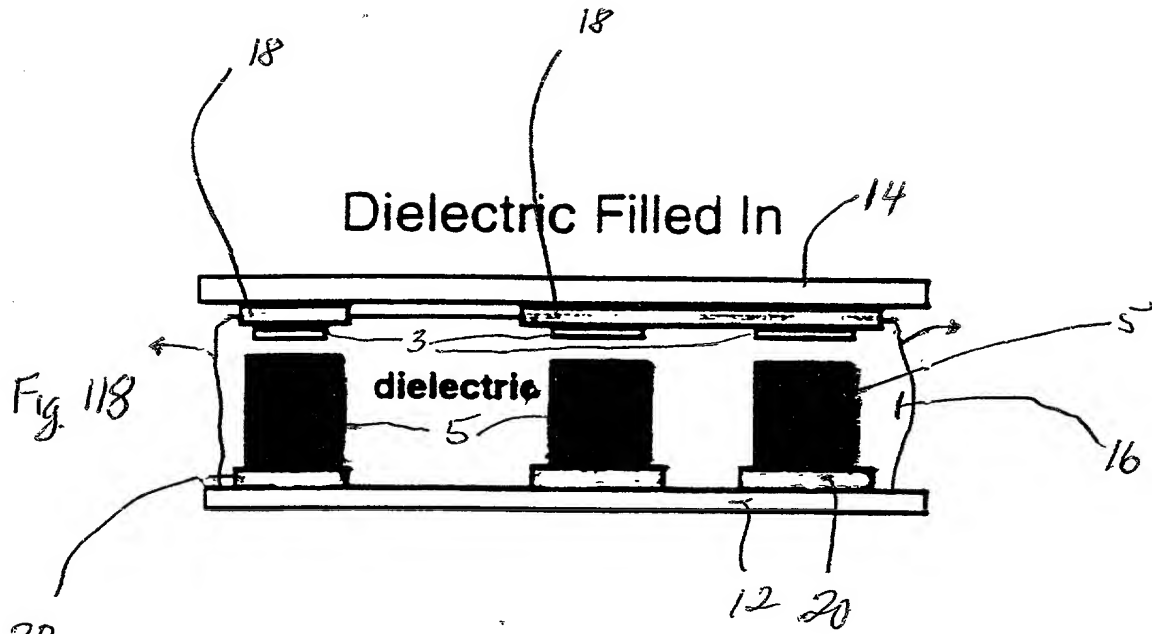


Fig 117

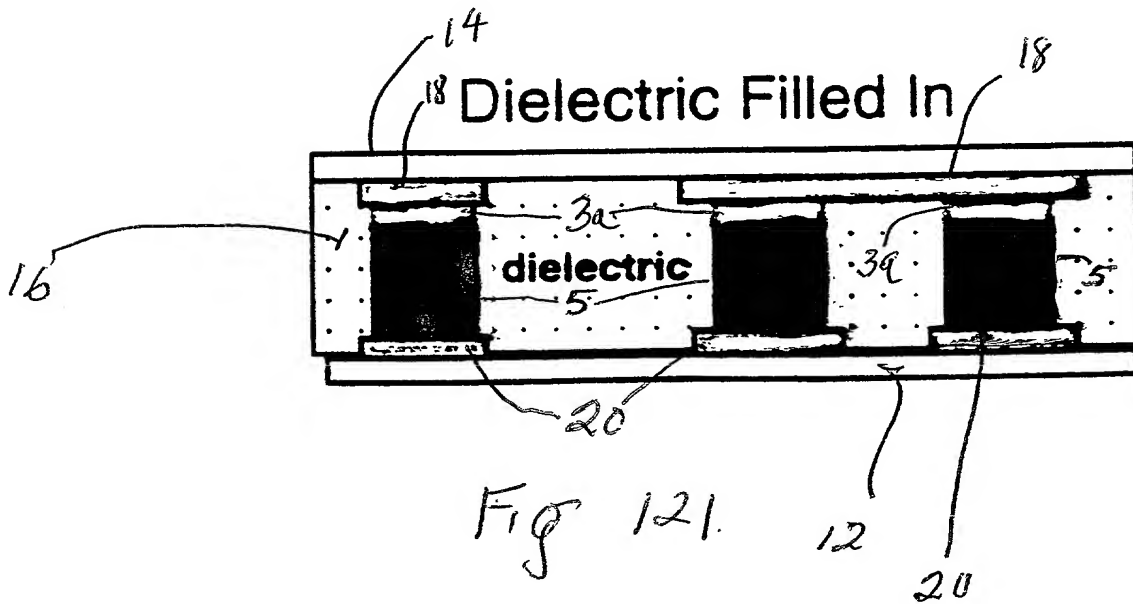
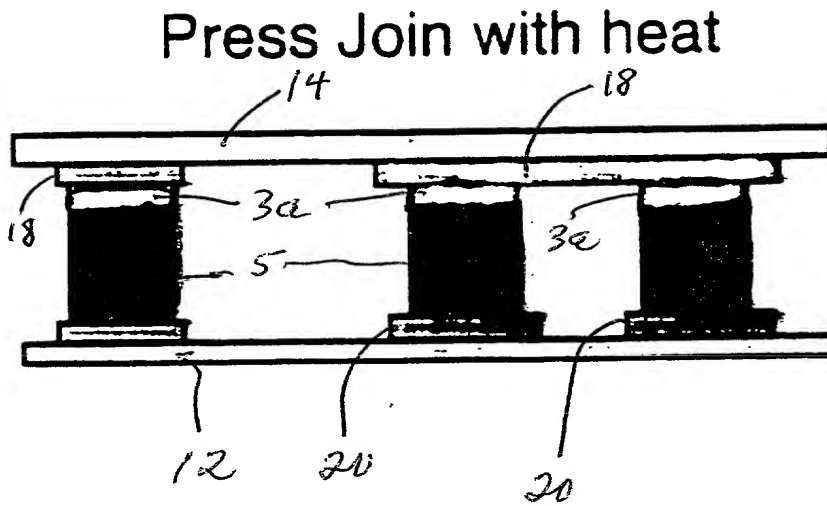
10065495 030103 201020 55495001





1006454-020702

Fig. 120



1006492 020102

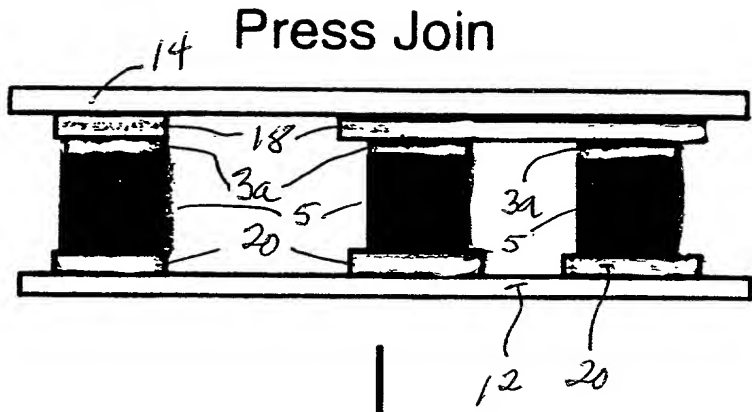


Fig 122.

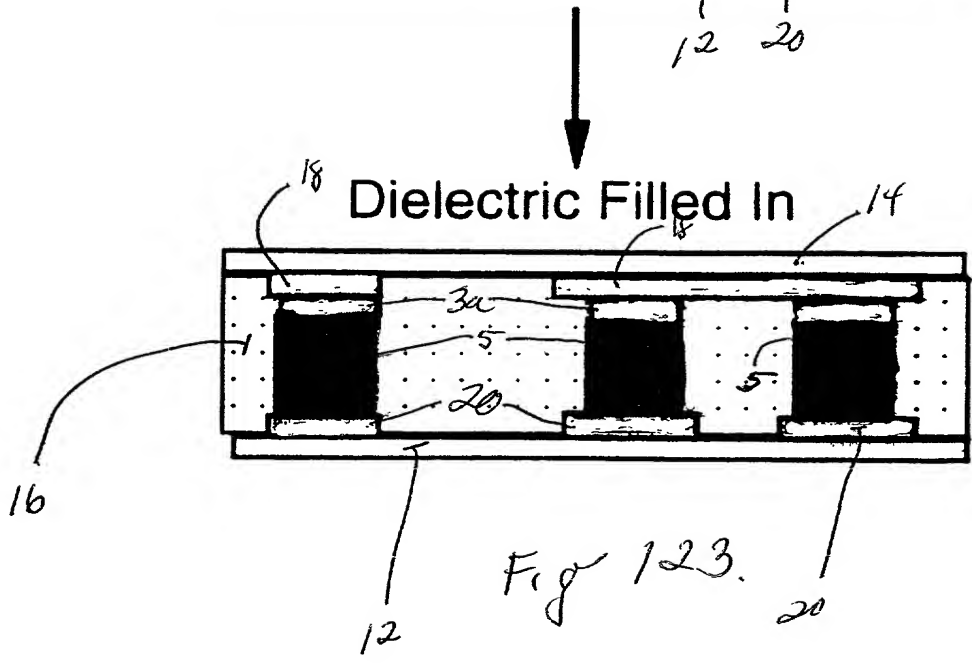


Fig 123.

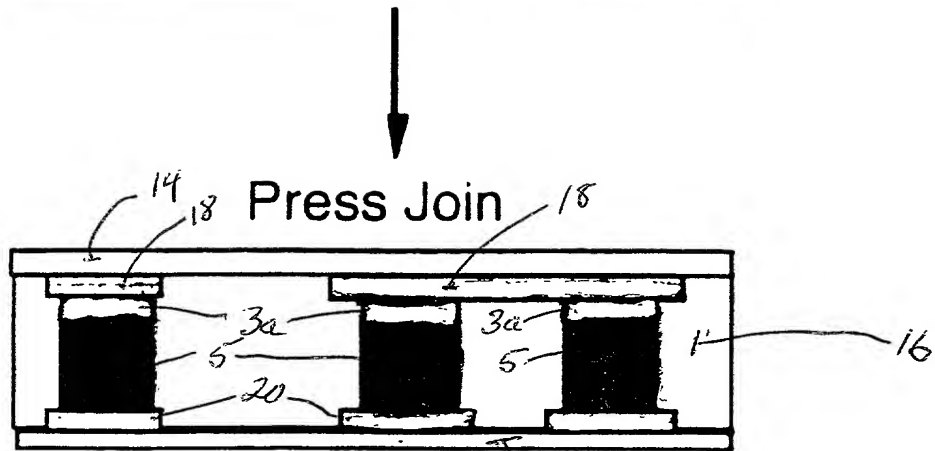
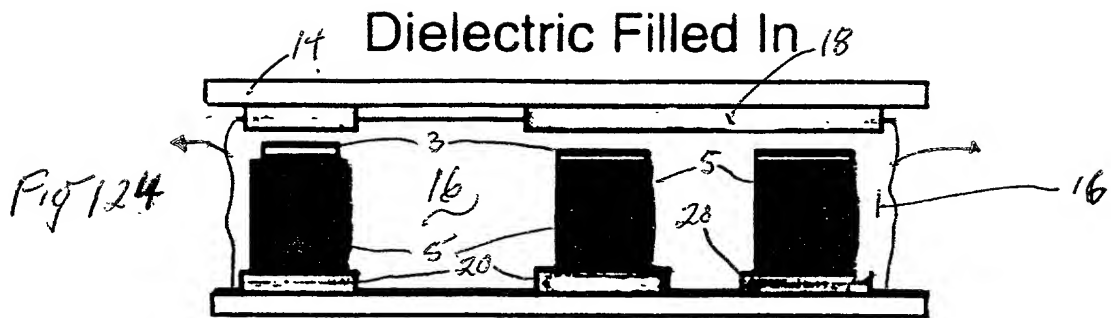


Fig 125

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